Lawrence Berkeley Laboratory
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Materials & Molecular Research Division

FINAL REPORT OF RESEARCH ON $Cu_xS/(Cd,Zn)S$
PHOTOVOLTAIC SOLAR ENERGY CONVERTERS 3/77 - 9/79

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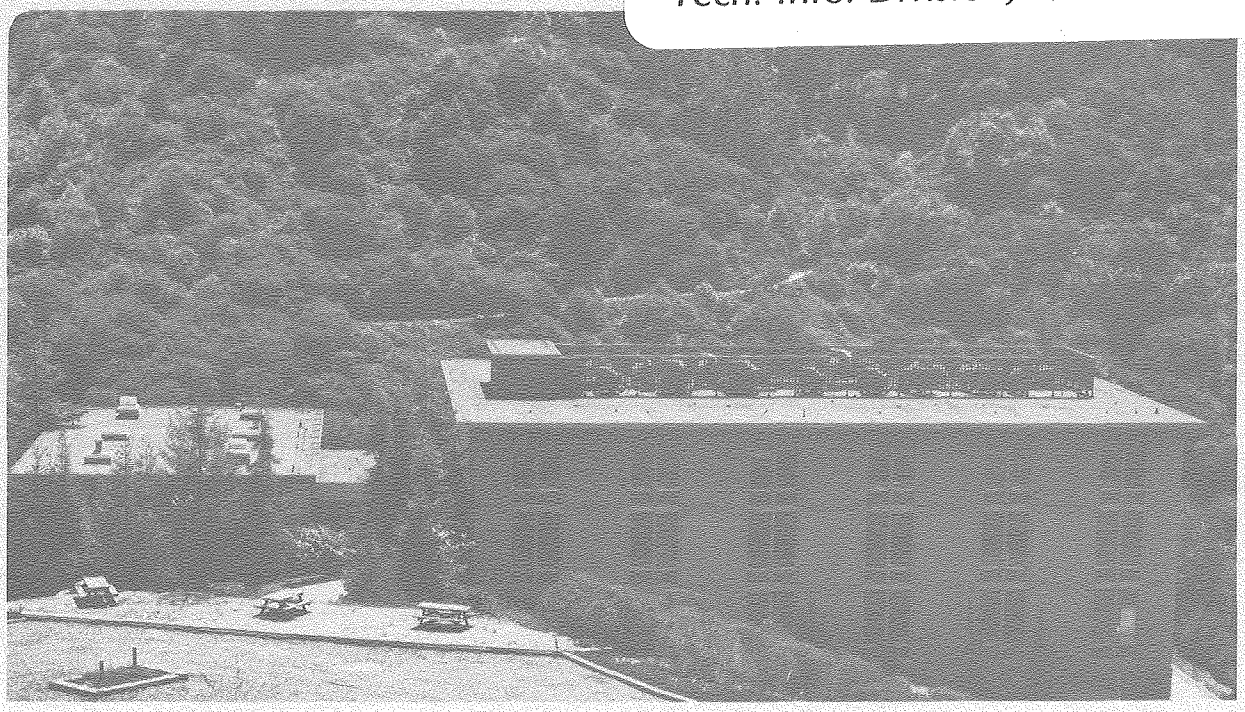
March 1980



Prepared for the U.S. Department of Energy under Contract W-7405-ENG-48

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Final Report of Research on $Cu_xS/(Cd,Zn)S$ Photovoltaic Solar Energy Converters

3/77 - 9/79

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1. Abstract

The objective of this program was to better understand the factors affecting the operation of CdS/Cu_xS and (Cd,Zn)S/Cu_xS photovoltaic cells. The approach was to systematically study the single crystal heterojunction so as to eliminate the complicating effects of grain boundaries. Single crystal CdS and (Cd,Zn)S thin films were deposited onto both GaAs and Ge substrates by a hot-wall vacuum deposition technique. These grown films were studied using X-ray diffraction, SEM-EDAX, TEM and Hall Effect experiments. Information concerning the effects of varying processing parameters on the chemical and structural nature of the deposited films was obtained. Detailed TEM studies revealed the presence of different dislocation structures which can affect the cell performance. Heterojunctions with Cu_xS were formed by the solid-state ion-exchange method and reactive sputtering (performed by the Lawrence Livermore Laboratory). Current-voltage and spectral response measurements of these cells were performed. The relationship between structural information and cell operation was studied. Suggestions for further work are outlined.

2. Introduction

2.1 Objective

The objective of this program was to investigate the Cu_xS/(Cd,Zn)S photovoltaic cell in order to better understand the factors that may be affecting its conversion efficiency. This has involved a detailed study of the growth and characterization of (Cd,Zn)S thin films and their heterojunction with Cu_xS.

2.2 Background

The Cu_xS/CdS thin film solar cell offers the advantages of both low cost material and low cost processing technology. The large-scale terrestrial use of the CdS cell has been delayed, however, by at least two major problems: relatively low efficiency and uncertain device lifetime. Ameliorating these two problems has been the object of several research programs both in Europe and the United States within the past decade.[1] Although there has been some success in these aims, present day cadmium sulfide cells remain less than 10 percent efficient and possess no longer than about a 20-year expected life.

A perturbation of the CdS cell is the replacement of the n-type side of the junction by (Cd,Zn)S. The addition of ZnS to form the continuous solid solution (Cd,Zn)S is expected to have several beneficial results, including (1) higher open-circuit voltage, meaning higher efficiency, (2) greater stability because of the decreased copper diffusivity in the mixed crystal (Cd,Zn)S, and possibly (3) higher short-circuit current because of a better lattice match at the interface. Initial studies performed on bulk single crystal[2] and polycrystalline[3] (Cd,Zn)S thin films have shown the expected

increase in open-circuit voltage. However, a decrease in short-circuit current with the addition of ZnS, was observed for the polycrystalline cells. In forming the Cu_xS layer by a conversion process the presence of grain boundaries in polycrystalline material results in a very complex interface. This presents a very difficult problem in attempting to analyze the electrical, chemical and structural nature of the heterojunction. Our approach has been to form a more simple planar interface by studying single crystal (Cd,Zn)S thin films and their heterojunctions.

2.3 Approach and Methods

In order to eliminate the complicating effects of grain boundaries, single crystal (Cd,Zn)S thin films have been grown. A hot-wall vacuum deposition technique was employed for the epitiaxial growth of (Cd,Zn)S closely paralleling the vacuum evaporation method used for conventional CdS thin film cells. The formation of the Cu_xS layer was accomplished by two methods: (1) conversion of part of the (Cd,Zn)S layer by a solid state ion exchange reaction, or (2) reactive sputtering performed by the Lawrence Livermore Laboratory.[4] The grown films and completed heterojunctions have been studied in a variety of ways using scanning electron microscopy with an energy dispersive x-ray analyzer (SEM-EDAX), x-ray diffraction and transmission electron microscopy (TEM). Electrical and optical measurements performed include Hall Effect experiments, current-voltage characteristics using a low frequency curve tracer, and spectral response measurements using a microprocessor-controlled apparatus.

3. (Cd,Zn)S Film Growth and Characterization

3.1 Experimental Methods

In order to obtain single crystal (Cd,Zn)S thin films for test devices a hot-wall vacuum deposition technique was adopted. Results from these growth experiments should be applicable to vacuum evaporated polycrystalline films. The design of the growth apparatus was modified from that of Behrndt and Moreno[5] to include separate sources for simultaneous and/or sequential evaporation of ZnS and CdS (the difficulties experienced with single source evaporation of (Cd,Zn)S has been reported by L. C. Burton, T. L. Hench and J. D. Meakin[6]). One baffle was placed between the two sources to prevent cross contamination and another between the sources and substrate to prevent spitting from the evaporating charges. A longitudinal cross section of the apparatus is shown in Fig. 3.1. Chromel-alumel thermocouples were placed against the alumina cylinder wall and substrate holder to monitor temperatures. The temperatures of the two individual sources were controlled by varying the power delivered by separate constant current power supplies. The mass of the ZnS and CdS charges were measured before and after each deposition run to give values for a normalized growth rate. A number of appropriate modifications were made later to the growth apparatus in order to achieve the desired results and are discussed in the following sections.

In operation the vacuum system containing the hot-wall apparatus is pumped down into the 10^{-6} torr range and the cylinder and substrate are heated separately to 400-600°C. The substrate holder is

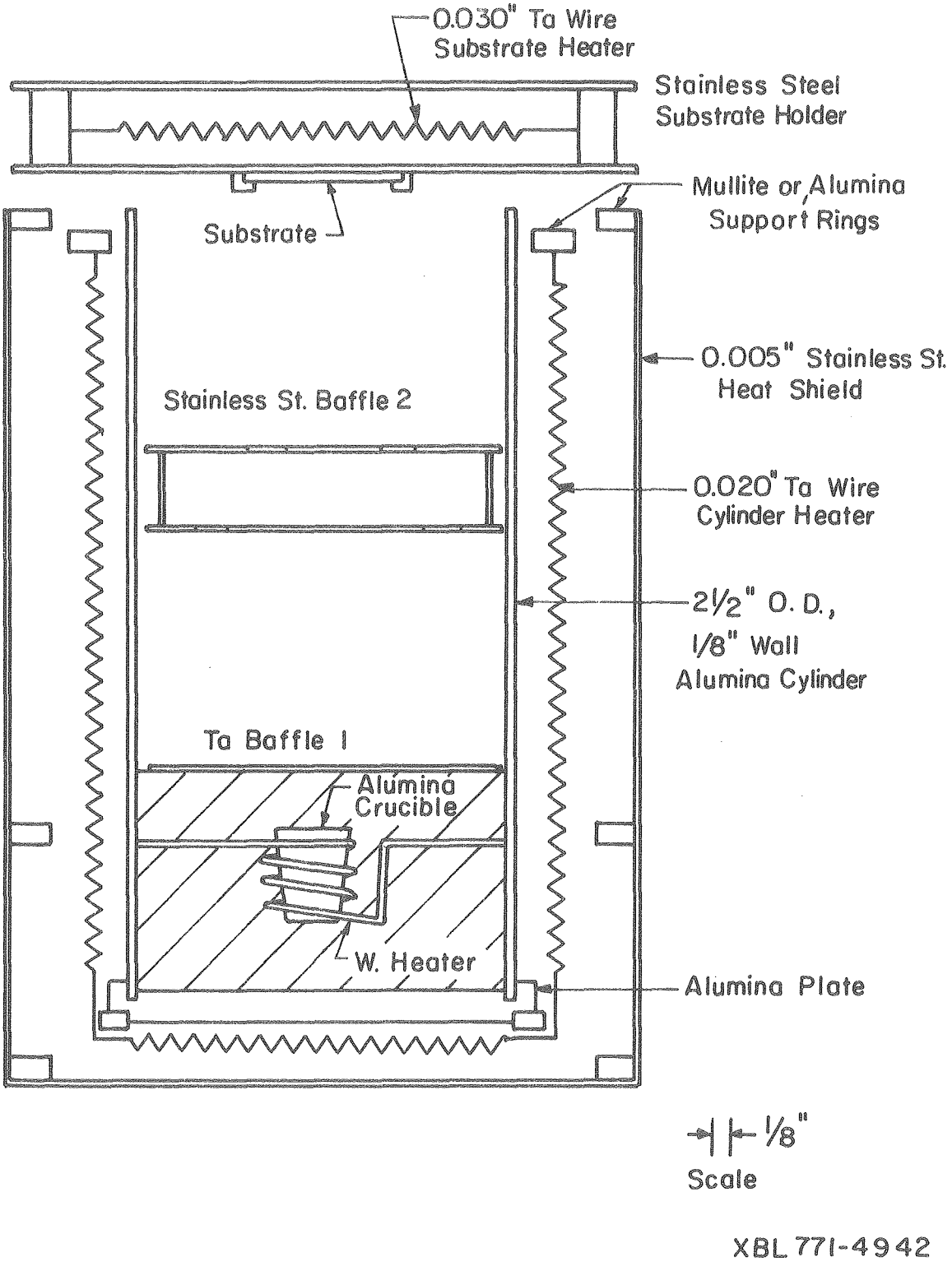

0.030" Ta Wire
Substrate Heater
Stainless Steel
Substrate Holder
Mullite or Alumina
Support Rings
Substrate
0.005" Stainless St.
Heat Shield
Stainless St. Baffle 2
0.020" Ta Wire
Cylinder Heater
2½" O. D.,
1/8" Wall
Alumina Cylinder
Ta Baffle 1
Alumina
Crucible
W. Heater
Alumina Plate
1/8"
Scale
XBL 771-4942

Figure 3.1

then lowered into position on the cylinder and allowed to equilibrate to the desired deposition temperature. The substrate is maintained at a temperature lower than the other parts of the growth chamber so that when the two sources are turned on, most of the vapor species will condense on the substrate and substrate holder. During the deposition the power to the sources and the temperatures of the cylinder wall and substrate are monitored.

Both (111) and off-(111) GaAs surfaces were used for the hetero-epitaxial growth of (Cd,Zn)S because of the good thermal expansion and lattice parameter matches (see Table 3.1). (111) Ge substrates were also used and the substrate preparations developed for the different substrates are outlined in the individual Film Growth sections.

P. Cherin, E. L. Lind and E. A. Davis have found[7] that (Cd,Zn)S forms a continuous series of solid solutions over the composition range from CdS to ZnS. They also reported a definitive calibration for lattice constants in which the variation of lattice parameters with composition was found to obey Vegard's law. This relationship was used to determine the composition of the grown films by measuring the d-spacings obtained from x-ray diffractometer scans. The surface morphology and composition profiles were examined using the SEM with EDAX attachment. More detailed structural investigations were performed using the transmission electron microscope as described in Section 4.

Table 3.1 Semiconductor Properties

Material	Crystal Structure	Lattice Constant (Room Temp.) (Å)	Linear Thermal Expansion Coefficient (RT → 800°C) (10^{-6}/°C)	Electron Affinity (eV)
CdS	Wurtzite	a = 4.137[a] c = 6.716	⊥ c 5.0[b] ∥ c 2.5	4.5[d] 4.87[e]
ZnS	Zincblende	a = 5.409[a]	6.5 - 8.5[b]	3.9[f]
GaAs	Zincblende	a = 5.654[d]	6.72[b] 5.7 - 7.3[c]	4.07[d]
Ge	Diamond Cubic	a = 5.658[d]	6.2[b] 5.7 - 7.6[c]	4.13[d]

References:

a. W. L. Roth, in "Physics and Chemistry of II-VI Compounds, "pp. 127-128, M. Aven and J. S. Prener, Eds., North-Holland, Amsterdam (1967).
b. W. M. Yim and E. J. Stofko, J. Electrochem. Soc. 119, 381 (1972).
c. "Thermophysical Properties of Matter," Volume 12, Y. S. Touloukian, Ed., IFI/Plenum, New York (1970).
d. A. G. Milnes and D. L. Feucht, "Heterojunctions and Metal-Semiconductor Junctions," Table 1.2, p. 8, Academic Press, New York (1972).
e. J. A. Van Vechten, Phys. Rev. 187, 1007 (1969).
f. R. K. Swank, Phys. Rev. 153, 844 (1967). Surface value.

3.2 Film Growth Results

a. Initial Growth Experiments

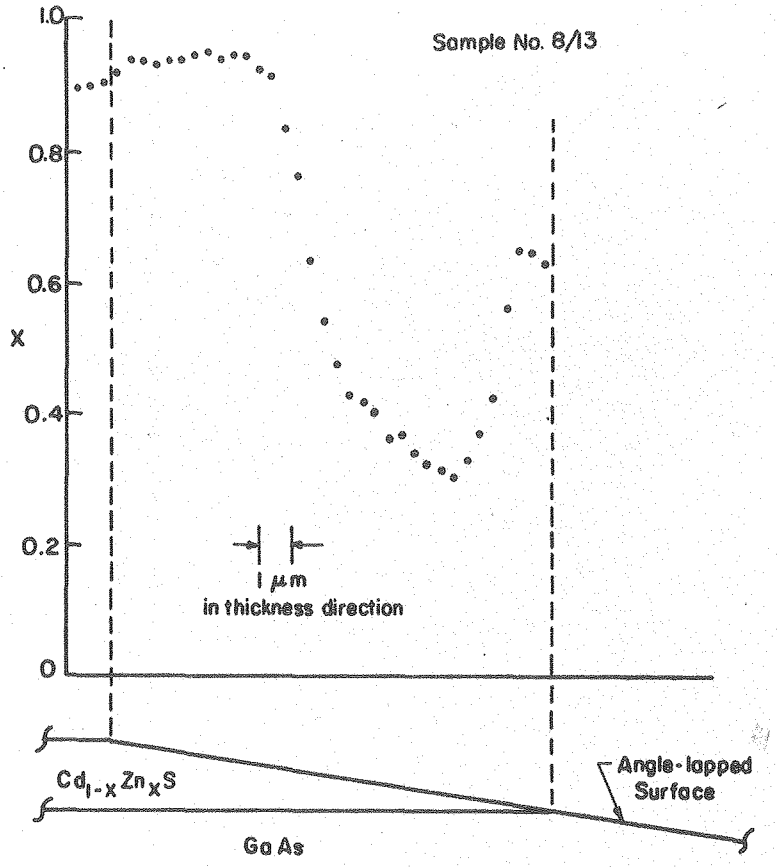
The initial growth runs were conducted using the hot-wall apparatus as shown in Fig. 3.1 to determine the conditions necessary for single crystal (Cd,Zn)S growth on (111) GaAs substrates. It was found that cross-heating between the evaporation sources in the growth chamber was negligible. Therefore, it was hoped that by determining the growth rates of CdS and ZnS separately these results could be used as a first approximation to the correct evaporation conditions for a given Cd-Zn ratio in a co-deposition. A very simple model was found to give a good fit to the growth of CdS deposits under several different growth conditions. However, it was then discovered that, although there was no thermal interaction of the sources, enough Zn vapor found its way around the baffles to the CdS source to drastically affect the CdS vaporization rate. This finding has also been reported recently by researchers at the University of Delaware, Institute of Energy Conversion.[6] To circumvent this problem, an iterative procedure was used in which a given combination of source temperatures was tried and the resulting film composition determined from the x-ray diffractometer peaks. The temperatures were then changed in the appropriate directions for the next deposition in order to approach the desired composition.

In addition to the x-ray diffractometer measurement which gave a fairly precise determination of the surface layer composition and an idea as to the degree of polycrystallinity, the film composition as a

function of depth was measured by two other means. The more precise of these was the electron microprobe which was used to scan an angle-lapped section of the film. Figure 3.2a shows the results of such a scan on an early film having large composition gradients. When reasonable care was taken, this kind of measurement gave relative accuracies of the order of 1 percent.

A more qualitative, but also much more readily performed, measure of the transverse film composition was provided by the energy dispersive x-ray analyzer (EDAX) in the scanning electron microscope (SEM) with the vertical deflection of the beam-scan turned off. Using this technique, one could observe the composition profile at a cleaved edge of the film. Figure 3.2b is an example of such an experiment performed on the same sample as shown in Fig. 3.2a. Seen in Fig. 3.2b is a triple exposure of the same area of the specimen, at the same magnification, but in two operating modes. The two white lines graphically depict the film composition versus depth, i.e., the vertical displacement is proportional to the weight percent of the element being analyzed. The background "picture" is a normal SEM micrograph taken after the line scans in which the darkened band shows where the electron beam was repeatedly swept for the composition analysis. Note that the electron microprobe and SEM-EDAX analysis are in excellent qualitative agreement.

Figures 3.3a and b show respectively an EDAX profile of the cleaved edge and a low-magnification SEM micrograph of the top surface of a later grown film. It can be seen that this film is much more



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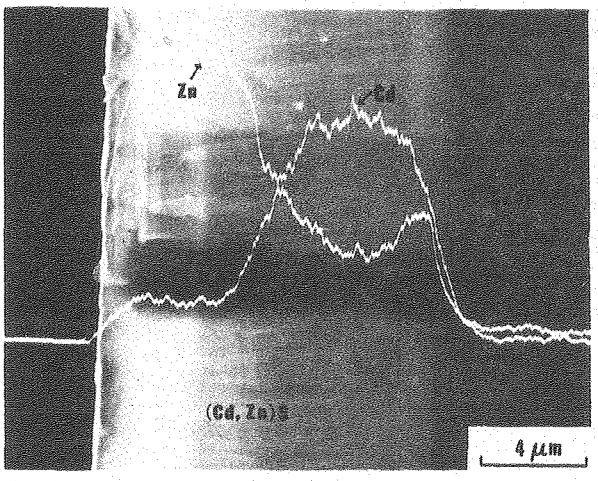

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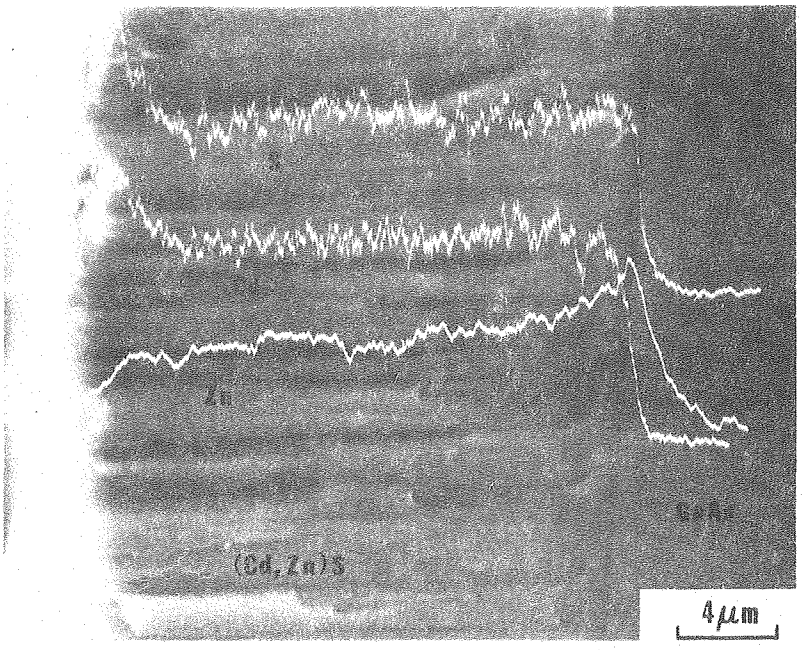
b

Figure 3.2



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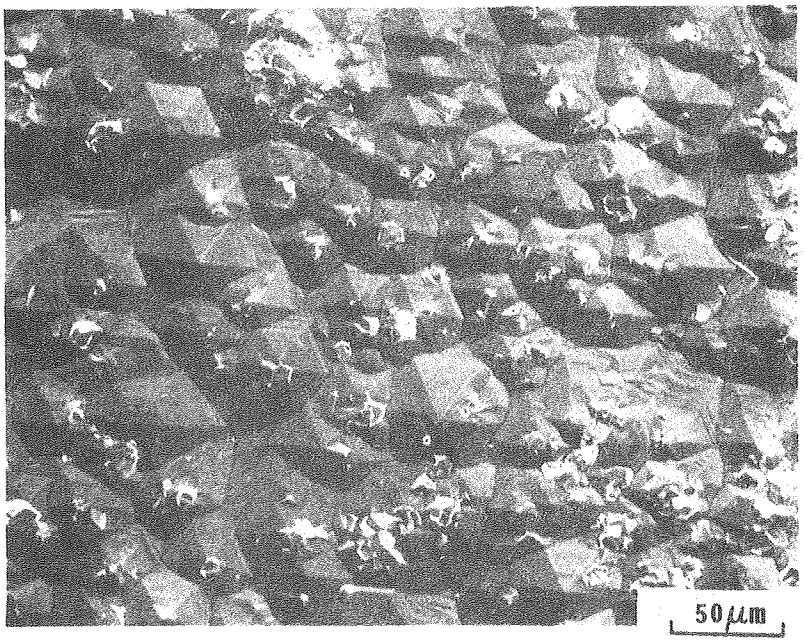

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Figure 3.3

nearly uniform than that of Fig. 3.2. The x-ray diffractometer scan of the sample of Fig. 3.3 showed evidence of some polycrystallinity in the film. It was discovered that the irregular shapes visible primarily on the tips of the hexagonal pyramids of Fig. 3.3b were responsible for the extra x-ray peaks. The morphology of the cleaved surface suggested that the misoriented grains existed only at the top surface of this sample.

Table 3.2 summarizes the experimental conditions and results for this group of films. The large scatter in thickness of the films grown under apparently similar conditions was thought to be due to escape of part of the charge at the seam between the hot-wall cylinder and the bottom end-plate. This view was supported by the observation that the background pressure outside the cylinder on some runs was much higher than for others where the resulting films were thicker.

One interesting result of these initial growth experiments concerns the differences in film growth on the Ga and As faces of the GaAs substrates. The GaAs wafers were supplied with one face polished, and this side was used for Films 10126 through 10266. However, when it was discovered that the wafers had all been polished on the same crystallographic face, the As $(\bar{1}\bar{1}\bar{1})$ or B-face, deposition on the opposite face, the Ga or A-face, was tried. It was found that growth on the Ga face has a greater tendency toward monocrystallinity and, further, it seemed to proceed at a higher rate (see the results for Film 11036 in Table 3.2). However, because of the difficulties

Table 3.2. Initial Film Growth Experiments

Run	ZnS Current (amps)	CdS Current (amps)	Run Duration (minutes)	Cylinder Temp. (°C)	Substrate Temp. (°C)	Crystallinity s = single p = poly	Thickness (μm)	Composition y in $Cd_{1-y}Zn_yS$ for (hkl)	Substrate
10126	46	30	60	600	495	p	30	(002) y = .15, .86 (103) y = .26 (004) y = .22	($\bar{1}\bar{1}\bar{1}$) As
10136	46	25	60	600	480	p	30	(002) y = .10, 1.0 ZnS (102) y = .08 (103) y = .10	($\bar{1}\bar{1}\bar{1}$) As
10156	43	25	60	600	485	–	–	Non-Uniform	($\bar{1}\bar{1}\bar{1}$) As
10186	41	23	60	600	470	p	~ 24	(002) y = .13 (102) y = .20 (103) y = .15 (104) y = .10	($\bar{1}\bar{1}\bar{1}$) As
10206	37	20	90	600	460	p	7	(002) y = 1.0 ZnS (102) y = .31 (103) y = .29	($\bar{1}\bar{1}\bar{1}$) As
10246	37	20	90	550	420	s	~ 2	(002) y = 1.0 ZnS	($\bar{1}\bar{1}\bar{1}$) As
10256	39	23	90	550	420	s	~ 3	(002) $\bar{y}$ = 0.70 Broad X-ray peak	($\bar{1}\bar{1}\bar{1}$) As
10266	39	24	180	560	430	p	~ 11	(002) y = .80 (102) y = .28 (103) y = .29	($\bar{1}\bar{1}\bar{1}$) As
11036	39	24	110	560	430	p	10	(002) CdS (101) y = .10 (102) y = .13 (103) y = .13	($\bar{1}\bar{1}\bar{1}$) As
						p	10 – 45	(002) y = .10 (102) y = .12 (103) y = .15 (004) y = .15	(111) Ga (unpolished)
11056	39	24	110	560	430	p	12–20	(102) y = .10 (103) y = .11	(111) Ga (polished)
11096	37	22	180	560	420	"s"	<1–13	(002) y = .15 (002) y = .75	(111) Ga (polished)
11176	37	22	180	560	395	–	<1	–	Baffle 2 used
11226	38	22	180	600	450	s	<1	(002) ZnS (004) ZnS	(111) Ga (unpolished)

mentioned earlier, this latter result was less certain. This difference in growth behavior is possibly due to the difference in stacking sequence for films grown on A- or B-faces.

b. Growth on (111) Ga-face GaAs Substrates

In order to prevent the cross contamination of the CdS charge by the Zn vapor and also escape of the vapor at the seams, a quartz cylinder with integral baseplate and baffle was used for subsequent runs as shown in Fig. 3.4. The two sources, each containing a charge of sintered grains of CdS or ZnS (Orion Chemical Company 5-9 pure), had quartz wool plugs and Ta baffles within the alumina crucibles to reduce splattering. Also shown in Fig. 3.4 is a metal block (initially Cr-plated copper and later Mo) positioned on top of the substrate to act as a heat sink for the GaAs. A thermocouple was placed within the heat sink to monitor the substrate temperature.

The results and the experimental conditions for the growth runs on the (111) Ga face are summarized in Table 3.3. These films were mostly epitaxial single crystals, as determined by x-ray diffractometry (those with some polycrystalline growth had off c-axis diffraction peaks with intensities at least two orders of magnitude less than that of the (002) peak). The composition of the films was determined from the (004) d-spacing.

It was observed that the perimeter region of the deposited film, which was shielded from the growth chamber by the substrate holder, showed different contrast in the SEM than the rest of the mixed crystal. This can be seen in Fig. 3.5a which is a micrograph of the

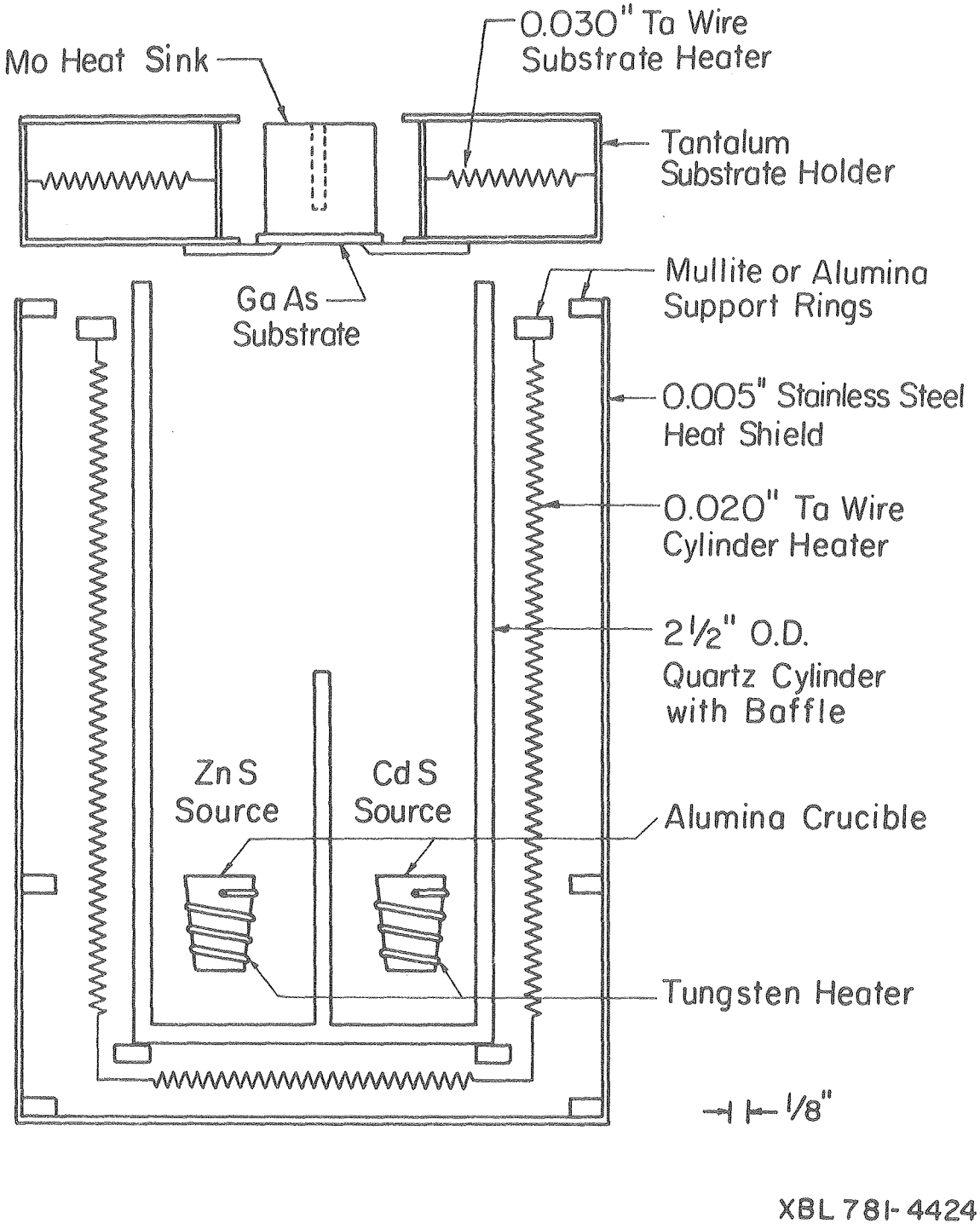
Mo Heat Sink
0.030" Ta Wire
Substrate Heater
Tantalum
Substrate Holder
Ga As
Substrate
Mullite or Alumina
Support Rings
0.005" Stainless Steel
Heat Shield
0.020" Ta Wire
Cylinder Heater
2½" O.D.
Quartz Cylinder
with Baffle
Zn S
Source
Cd S
Source
Alumina Crucible
Tungsten Heater
⊣ ⊢ 1/8"
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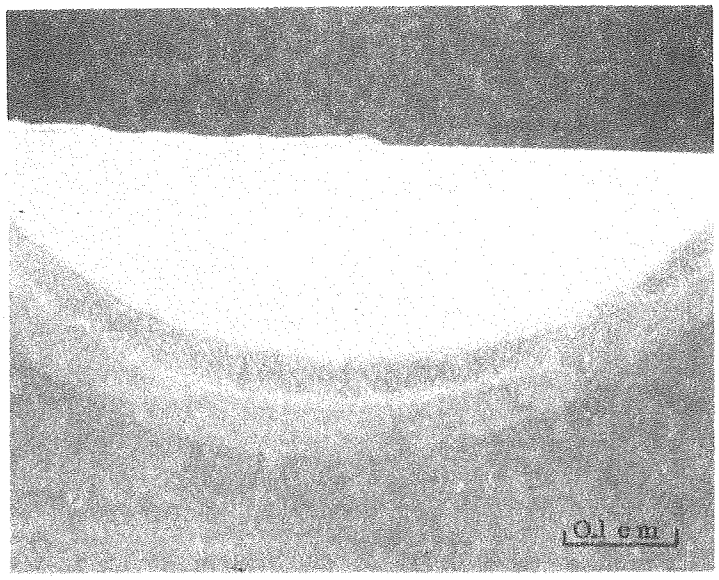
Figure 3.4

Table 3.3. Film Growth Experiments on (111) Ga-Face Substrates

Run	ZnS Power (watts)	CdS Power (watts)	Run Duration (minutes)	Cylinder Temp. (°C)	Substrate Temp. (S.S.) (°C)	ZnS Rate R_{ZnS} (mmole/hr)	CdS Rate R_{CdS} (mmole/hr)	ZnS Mole Fraction	θ (R_{ZnS}/R_{Total})	Thickness τ (μm)	$d\tau/dt$ (Å/sec)	Growth Rate, g (Å/μmole)
2047	304	120	60	550	(430)	6.05	13.31	0.29	.312	37.5	104.2	19.37
2097	343	102	30	560	(430)	8.17	16.72	0.29	.328	5.2	28.89	4.18
2107	400	99	60	560	(440)	14.62	14.06	0.90	.510	15.0	41.67	5.23
2167	395	96	60	510	(450)	10.38	10.65	0.90	.493	5.7	15.83	2.71
3037	267	96	60	560	(445)	3.83	10.0	0.24	.277	8.0	22.22	5.79
3297	225	93	60	560	(440)	2.64	13.80	1.00	.161	2.0	5.56	1.22
4017	269	92	60	560	(455)	3.93	11.64	0.82	.253	1.0	2.78	0.64
4057	244	90	60	560	(465)	1.19	2.77	0.31	.301	1.0	2.78	2.53
4077	300	119	60	600	(500)	4.98	8.32	0.82	.374	2.5	6.94	1.88
4137	250	105	60	560	(420)	0.96	4.40	0.17	.180	6.3	17.5	11.74
4197	240	105	120	560	(420)	0.83	3.59	0.22	.187	9.0	12.5	10.18
4267	270	112	120	560	440	1.77	5.44	0.19	.245	23.0	31.94	15.94
5247	258	100	120	560	425	1.29	4.34	0.15	.230	17.0	23.61	15.1
6067	300	100	60	600	475	4.24	4.63	1.00	.478	<1.0	---	---
6077	260	102	60	600	470	2.11	8.24	0.24	.204	3.5	9.72	3.38
6147	262	102	60	600	420	1.98	5.54	0.27	.263	3.5	9.72	4.65
6167	266	105	60	600	460	1.66	9.61	0.19	.148	5.0	13.89	4.44
6177	190	88	90	600	330	0.41	5.25	0.11	.073	9.0	16.67	10.6
6207	182	89.6	90	600	460 → 400	0.53	5.30	0.11	.091	10.0	18.52	11.4
6217	212	89.6	90	600	490 → 420	0.88	5.92	0.17	.130	6.0	11.11	5.88
6237	212	89.6	90	600	340	1.15	4.76	0.17	.195	5.0	9.26	5.64
6277	199	89.6	90	600	340	---	3.72	0.07	---	12.0	22.22	---
7297	0	86.8	90	600	360	0	4.08	0	0	4.0	7.41	6.54
8107	215	89	90	600	340	0	7.06	0	0	15.0	27.78	14.16
8187	216	89.6	90	600	400	0.89	0	1.0	1.0	<1.0	---	---
8317	228	89.6	90	600	370	1.03	5.77	0.05	.135	21.6	40.0	18.47



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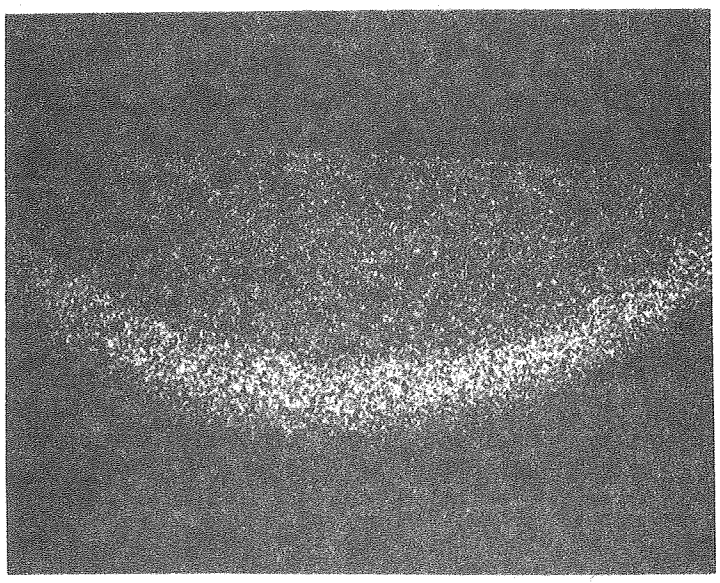

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Figure 3.5

top of a (Cd,Zn)S specimen which was cleaved for transverse compositional analysis. The x-ray mapping technique of the SEM-EDAX was used to show the origin of this contrast difference. In the x-ray mapping mode the concentration of an element is related to the density of dots in each area on the display screen. Figure 3.5b is such a map of the same specimen as in Fig. 3.5a with the x-ray analyzer set up to detect Cd. Enhanced concentration of Cd in the perimeter region can be seen. A more precise measurement by x-ray diffraction determined this area to be "pure" CdS. This result can be explained by the higher surface diffusivity of Cd compared to that of Zn.

It was found that no cross-contamination of evaporation charges occurred due to the integral baffle in the quartz hot-wall cylinder. This has resulted in far better processing control of the mixed crystal films and also in compositional uniformity. Figure 3.6 shows the x-ray line scans of the cleaved cross-section of a grown film for Cd, Zn and S which are seen to be relatively uniform through the film thickness.

The SEM was also used to characterize different surface morphologies of the mixed crystal films. Figure 3.7a shows the rough surface of a polycrystalline film. In contrast, the surface of a single crystal film with a high growth rate (Film 4267) is shown in Fig. 3.7b. In most of the deposited films cracks were observed. Fine randomly oriented cracks were found for Film 5247, as seen in Fig. 3.8. Long cracks propagating along the $\langle 11\bar{2}0 \rangle$ crystallographic directions were observed for Film 6077 (Fig. 3.9). Film growth over a

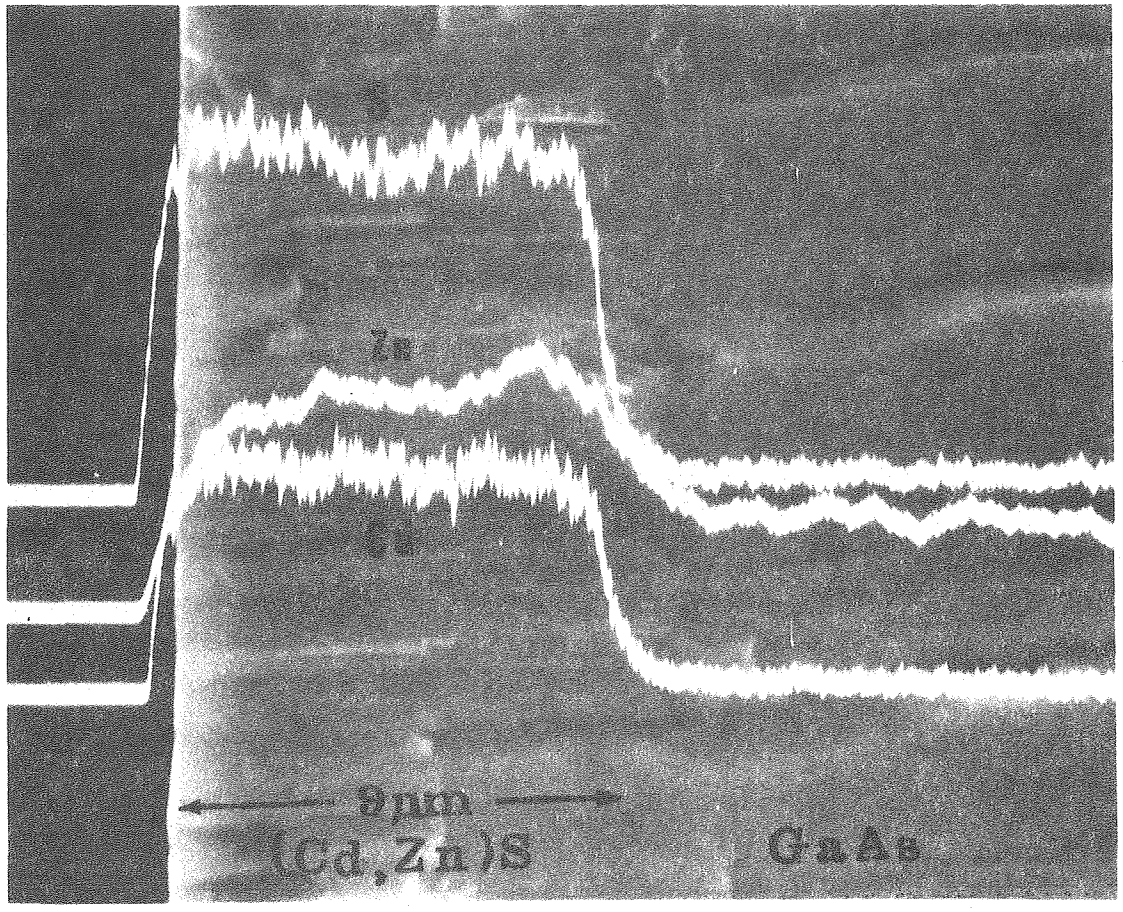

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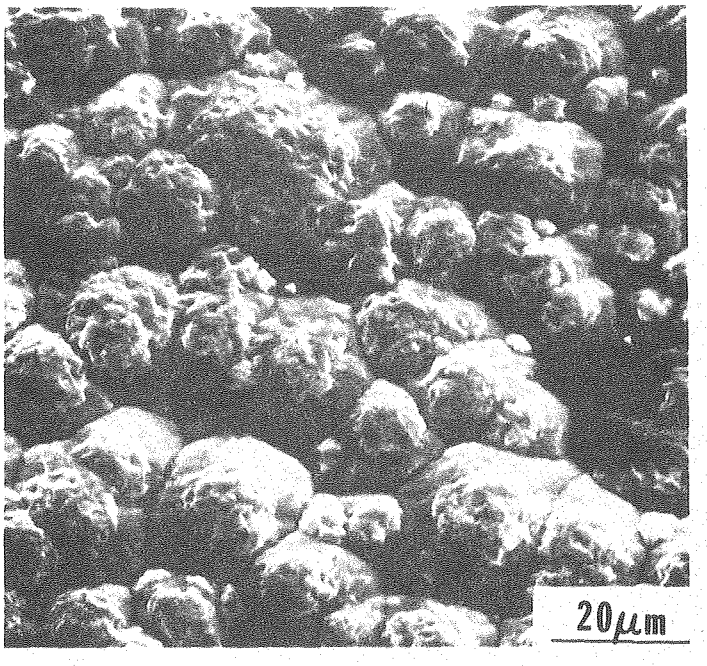
Figure 3.6



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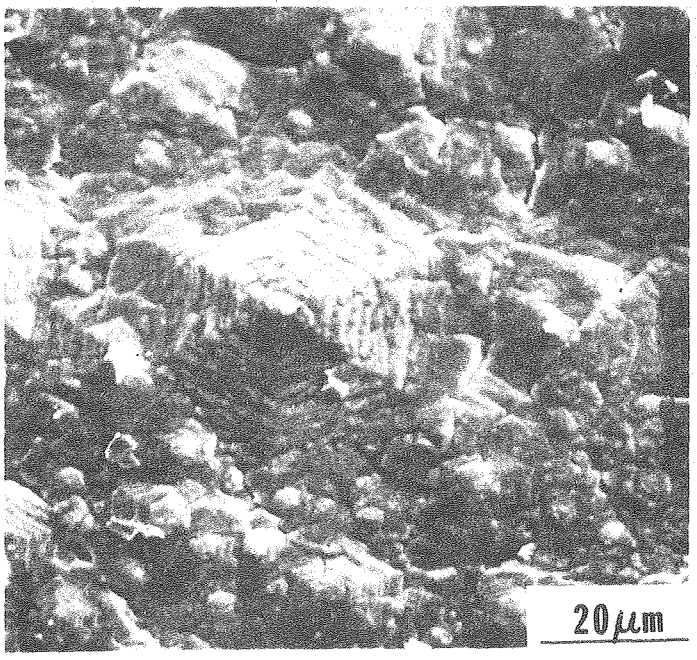

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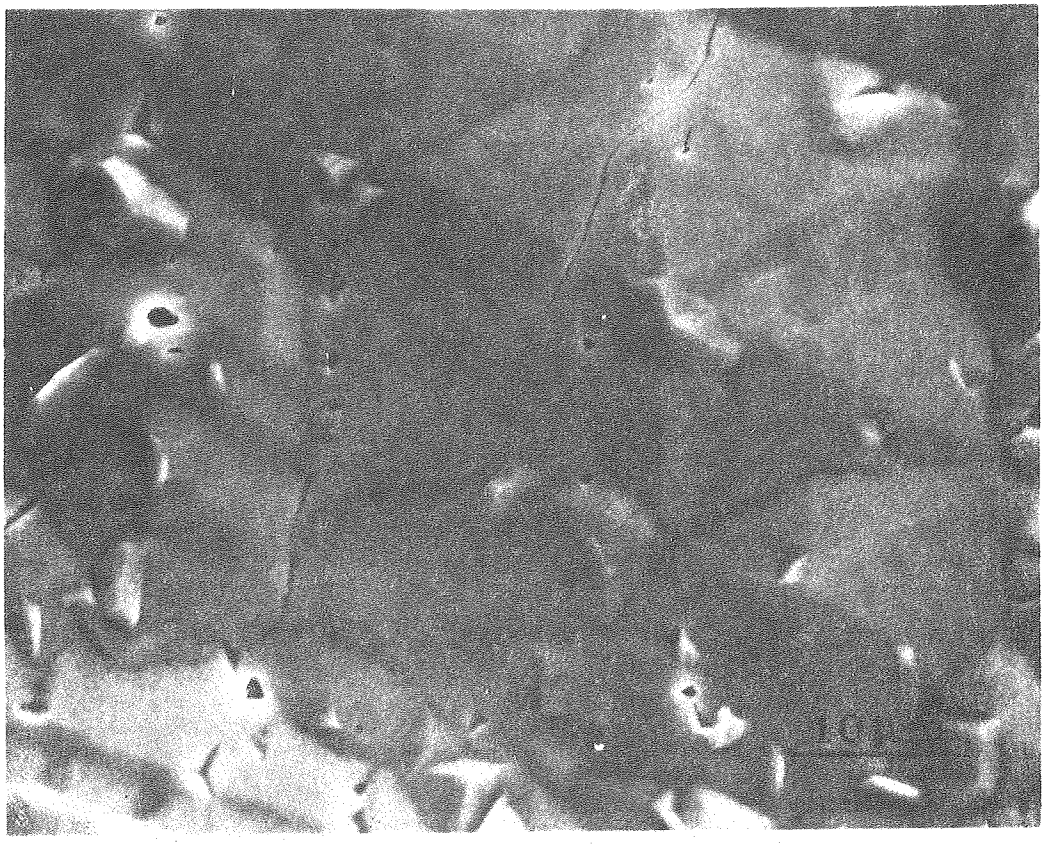
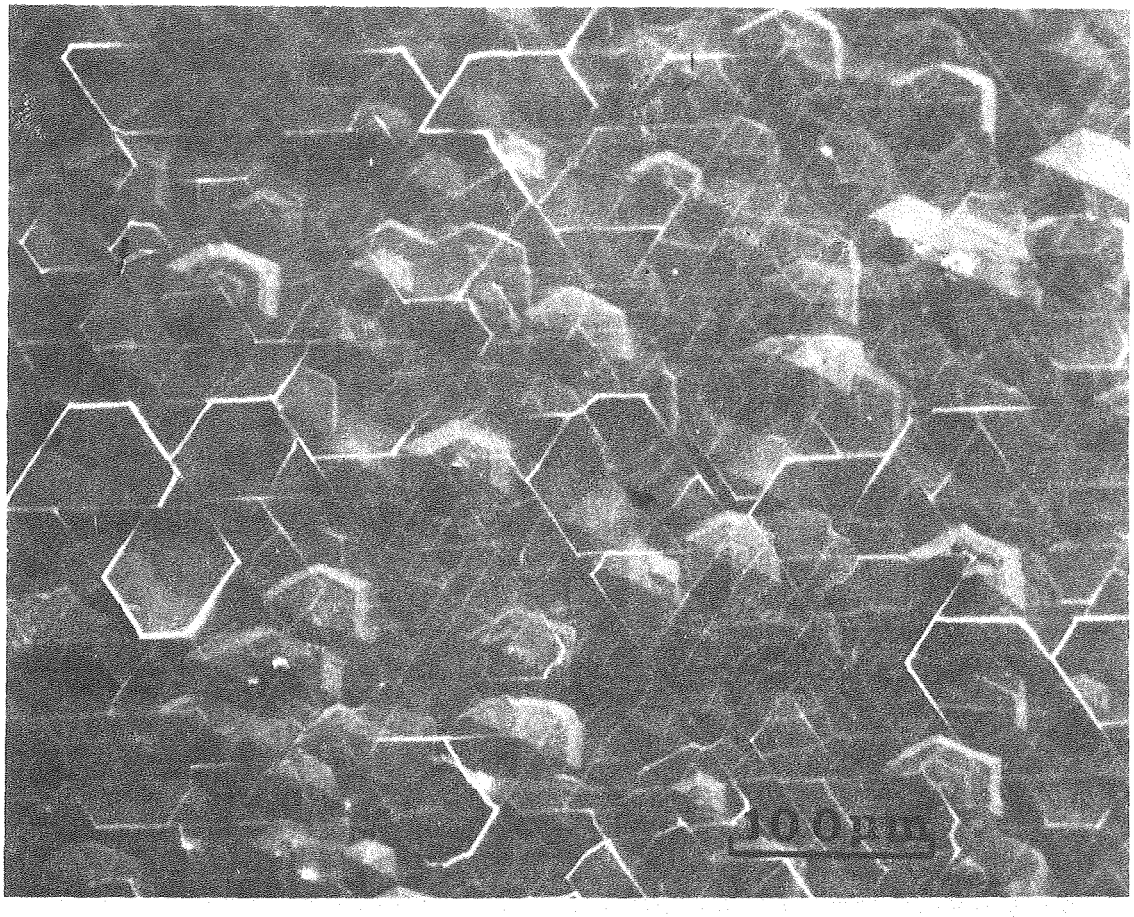
Figure 3.7



XBB 777-6726

Figure 3.8



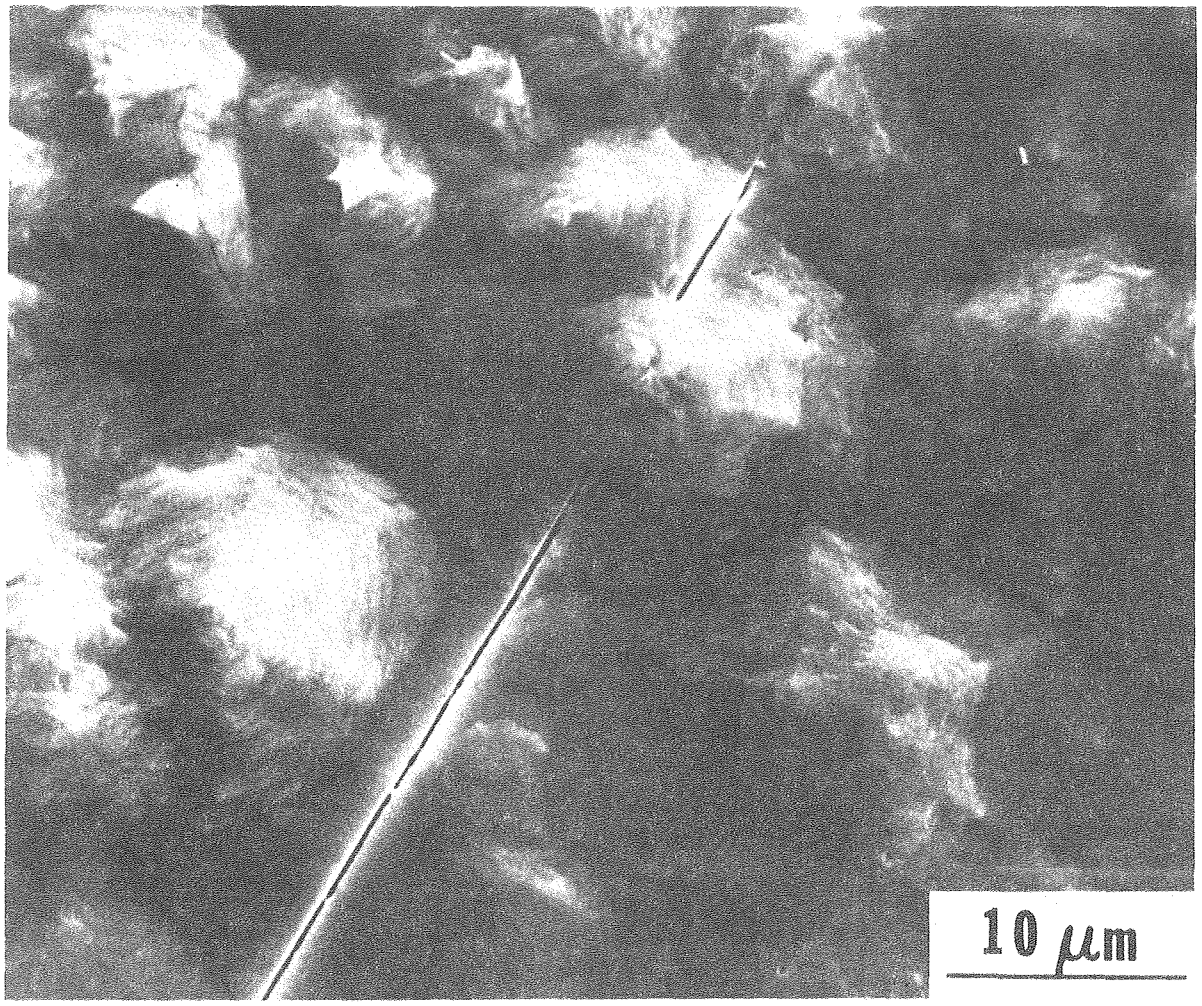
XBB 777-6725

Figure 3.9

crack, as seen in Fig. 3.10 (Film 5117), indicates that the cracks were formed early during crystal growth. Cracks have also been observed for (Cd,Zn)S films grown on (111) GaAs substrates by the close-space transport method.[8]

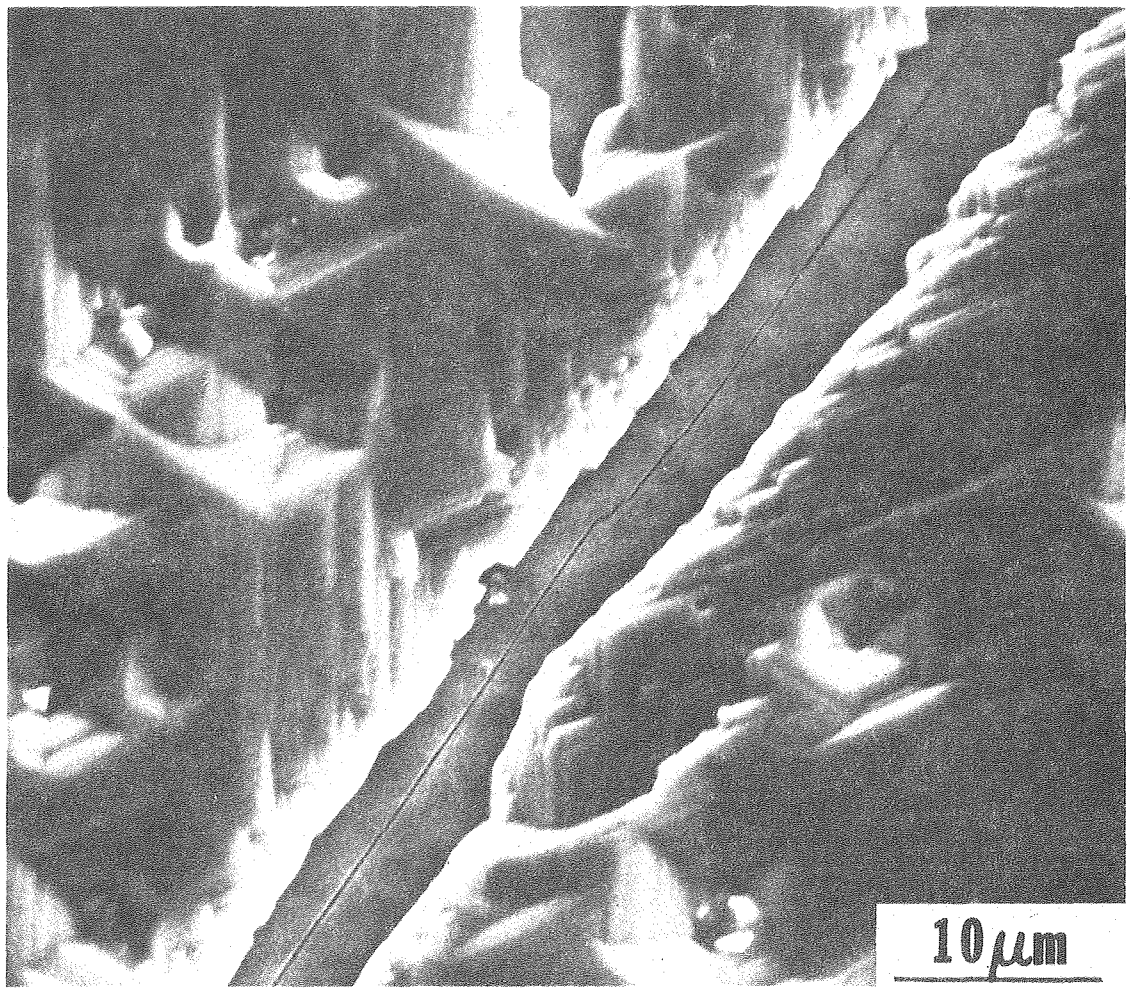
In an effort to determine the origin of these cracks, Film 4197 was polished and then etched for 30 seconds in ~50 percent $HCl:H_2O$. Figure 3.11 shows the result of this treatment and indicates that the cracks extend through the thickness of the (Cd,Zn)S film. X-ray diffraction analysis revealed that GaS was present under the film after the cracks were opened by etching, suggesting that a thin film of GaS forming between the GaAs substrate and mixed crystal may have been responsible for the development of these cracks. Further experiments were conducted to determine the origin of this problem as discussed in Section 3.2c.

The dependence of film composition and growth rate on the experimental parameters was also studied. Both the growth rate and composition were found to be extremely sensitive to the relative rates of evaporation of the ZnS and CdS charges. Figure 3.12 shows the variation of x, the ZnS mole fraction in the film, with θ, the ZnS fraction of spent charge. The data shown in this figure encompass substrate temperatures from 330 to 475°C, cylinder temperatures between 560 and 600°C and total charge loss rates from 3.96 to 28.68 mmole/hr. Almost all of the Ga-face films fall near the line shown in the figure. There is apparently a preferential incorporation of ZnS in the single crystal (0002) films. In spite of (or possibly because



XBB 776-6047

Figure 3.10



XBB 776-6046

Figure 3.11

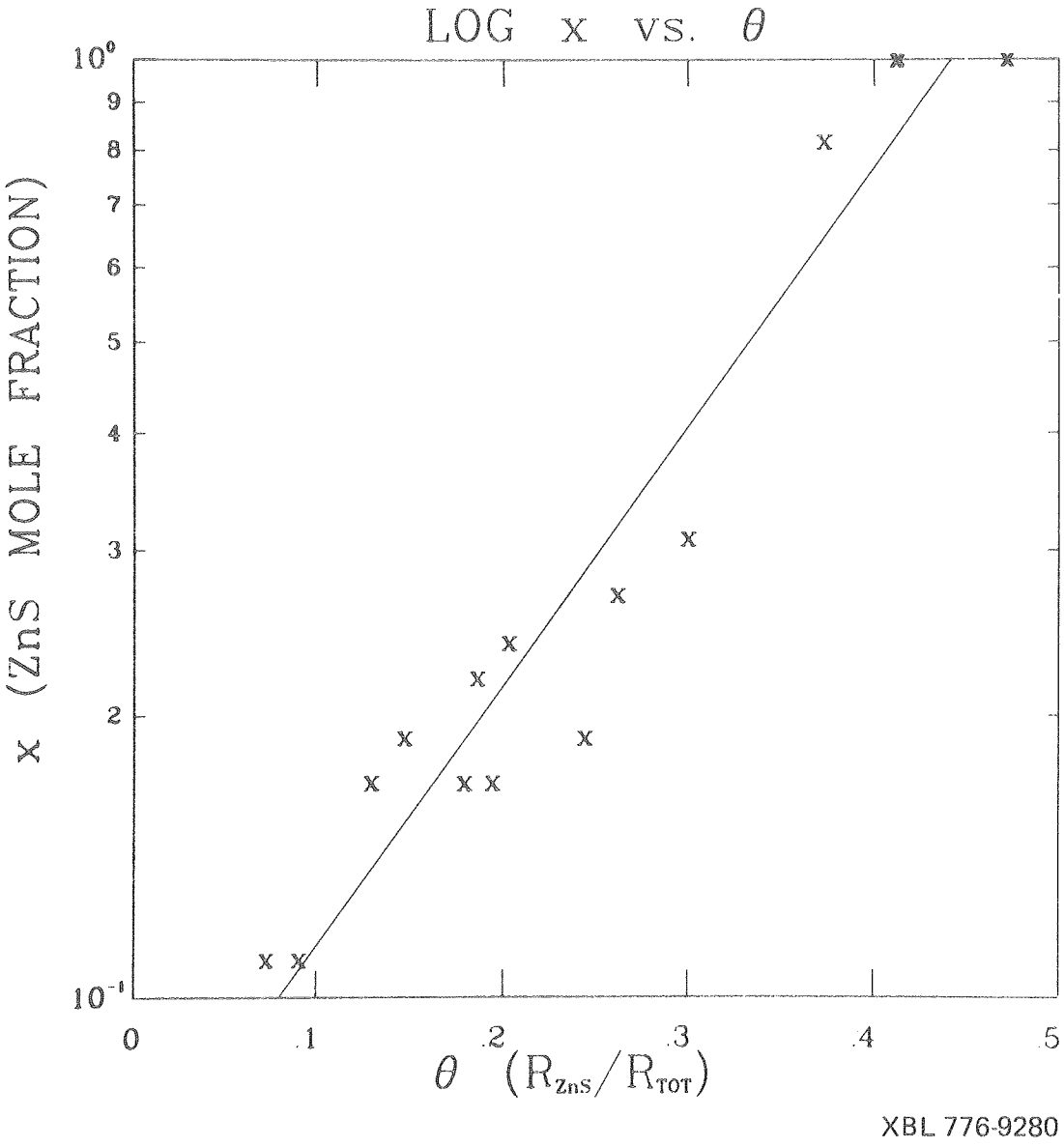

LOG x vs. θ
x (ZnS MOLE FRACTION)
10⁰
9
8
7
6
5
4
3
2
10⁻¹
0
.1
.2
.3
.4
.5
θ (R_ZnS/R_TOT)
XBL 776-9280

Figure 3.12

of) this preference, the normalized growth rate, i.e., the growth rate divided by the total charge loss rate, shows a rapid decrease with increasing θ as seen in Fig. 3.13. Figure 3.13 represents data for films grown with a 600°C cylinder temperature at various total charge loss rates and substrate temperatures. If the data of Fig. 3.13 are plotted vs. x, Fig. 3.14 is obtained, showing a somewhat weaker, but still remarkable, dependence of g on x. The mechanisms underlying this phenomenon are as yet not understood; however, there is perhaps a clue contained in the calculations of Gilmer and Bennema[9] based on computer simulations of crystal growth. They find an exponential dependence of growth rate on the step formation energy. Since the bond strength of ZnS is greater than that of CdS, one might expect an increase in the surface step formation energy of (Cd,Zn)S crystals as the ZnS fraction increases.

c. Effect of GaAs Substrate Preparation and Orientation

It was found that (Cd,Zn)S films grown on the (111) Ga face developed cracks propagating through the thickness of the film and also into the GaAs substrate. To eliminate this problem the effect of different etchants, substrate surface and substrate orientation on crack development was studied. These results are summarized in Tables 3.3 and 3.4A. The various substrate conditions examined were:

(1) (111) Ga face polished for ~ 10 sec on a microcloth saturated with chlorox (Films 5247 through 6277).

(2) (111) Ga face polished for ~ 30 sec on a microcloth saturated with 2 percent Br:CH_3OH (Films 7297 through 8317).

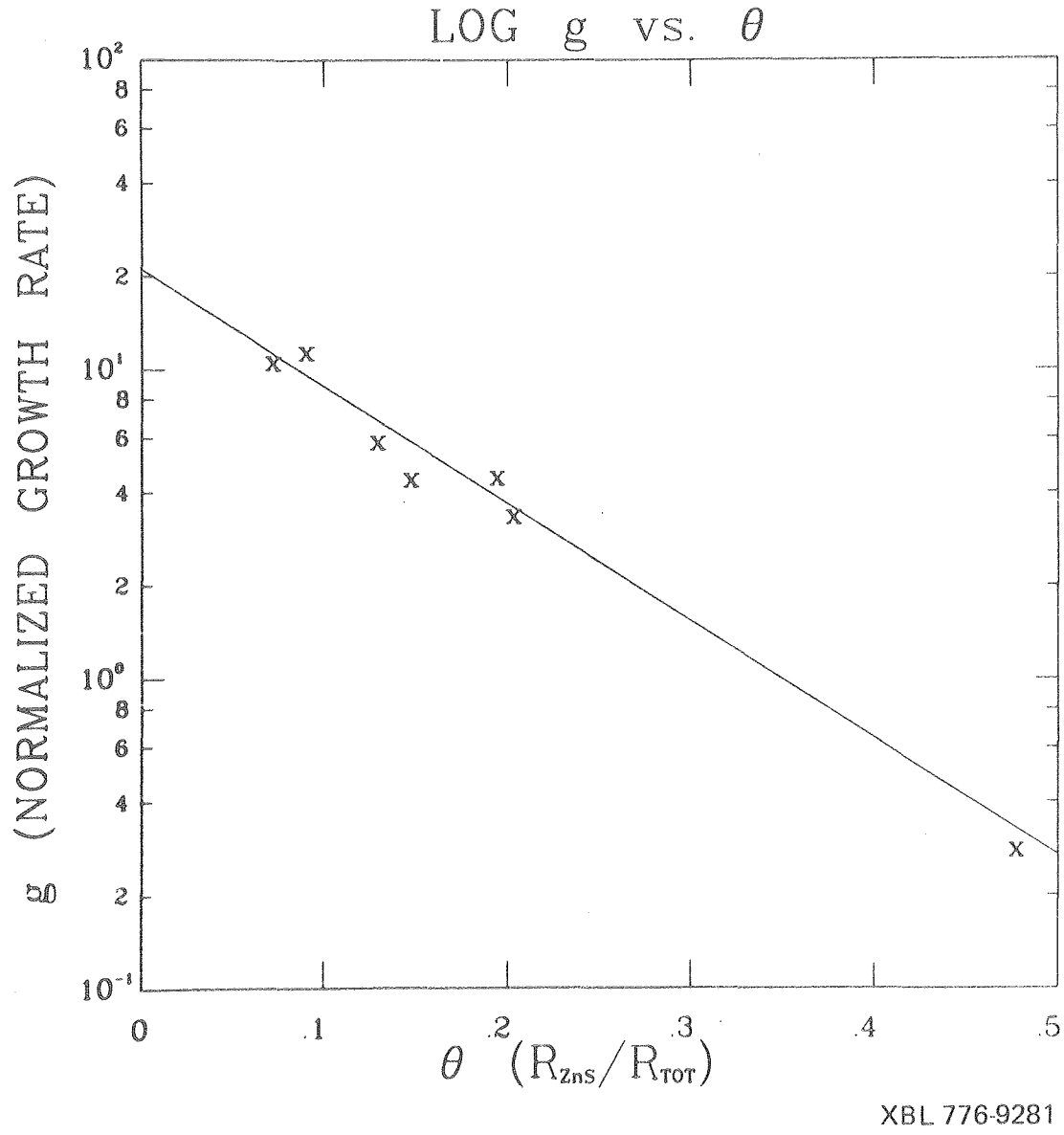


Figure 3.13

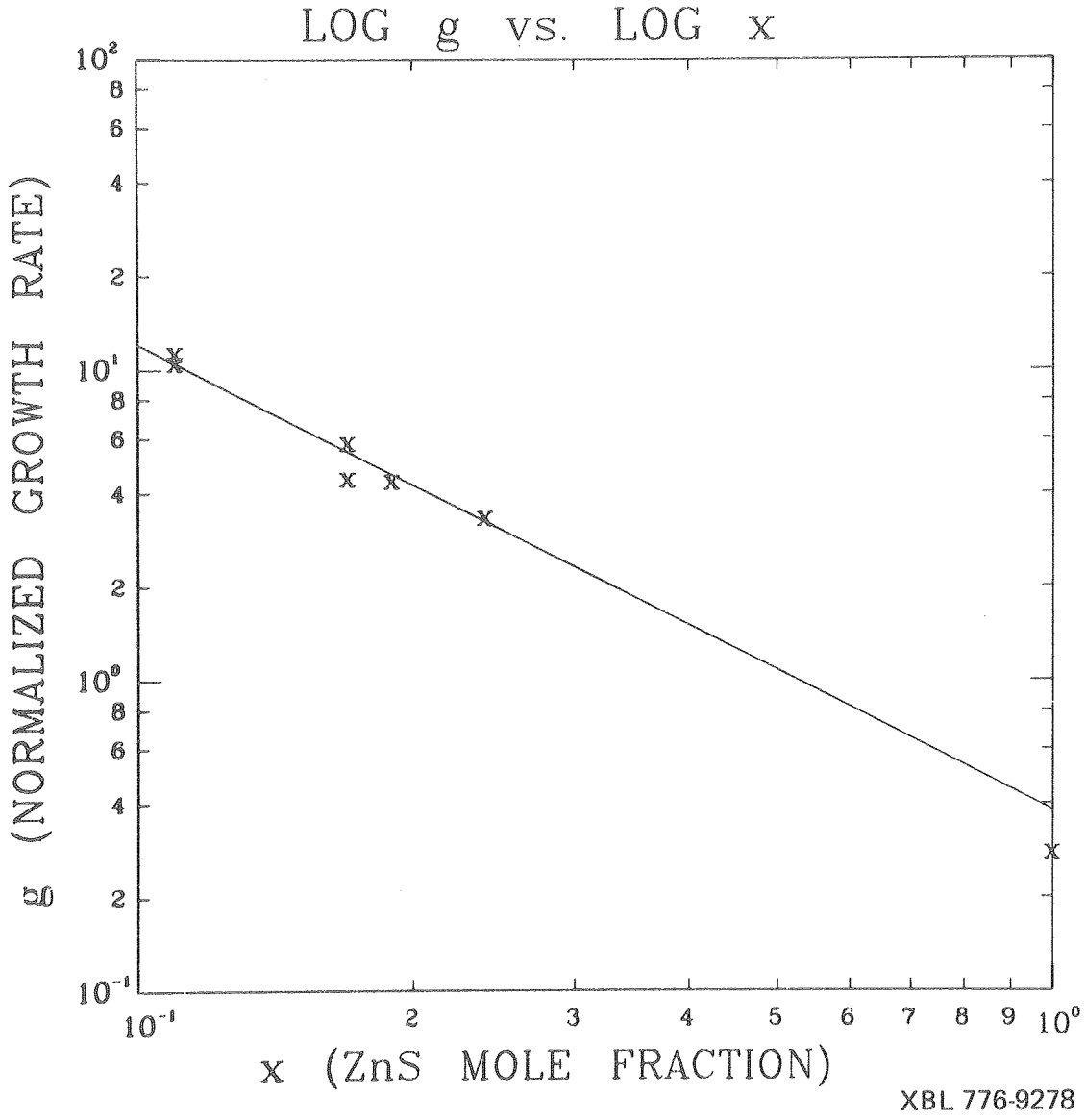

LOG g vs. LOG x
g (NORMALIZED GROWTH RATE)
x (ZnS MOLE FRACTION)
XBL 776-9278

Figure 3.14

Table 3.4A. Effect of GaAs Substrate Preparation and Orientation

Run	ZnS Power (watts)	CdS Power (watts)	Run Duration (minutes)	Cylinder Temp. (°C)	Substrate Temp. (°C)	ZnS Rate R_{ZnS} (mmole/hr)	CdS Rate R_{CdS} (mmole/hr)	ZnS Mole Fraction	θ ((R_{ZnS}/R_{Total}))	Thickness τ (μm)	$d\tau/dt$ (Å/sec)	Growth Rate g (Å/μmole)	Substrate
9017	0	136	30	590	385	0	13.22	0	0	20.0	111.1	30.25	$(\bar{1}\bar{1}\bar{1})$B
9067	0	120	30	585	400	0	8.25	0	0	10.0	55.55	24.24	$(\bar{1}\bar{1}\bar{1})$B
9077	232	102	60	600	410	0	8.31	0	0	27.5	76.39	33.11	$(\bar{1}\bar{1}\bar{1})$B
9097	232	78	60	600	380	0	5.67	0	0	18.0	50.00	31.75	Off $(\bar{1}\bar{1}\bar{1})$B
9107	232	65	60	600	410	0	2.64	0	0	6.6	18.33	24.96	Off $(\bar{1}\bar{1}\bar{1})$B
9127	236	67.5	60	600	420	0.72	3.27	0.05	0.18	18.7	51.94	46.92	Off $(\bar{1}\bar{1}\bar{1})$B
9197	225	60	60	600	420	0.78	2.87	0.05	0.21	15.0	41.67	41.14	Off $(\bar{1}\bar{1}\bar{1})$B
9207	232	57.6	60	600	420	0.70	2.56	0.05	0.21	13.3	36.94	40.81	Off $(\bar{1}\bar{1}\bar{1})$B
9297	250	60	60	600	420	0.75	2.33	0.09	0.24	5.0	13.88	16.22	Off $(\bar{1}\bar{1}\bar{1})$B
9307	225	58	30	600	400	0.68	2.00	0.03	0.25	8.0	44.44	59.69	Off (111)A
12067	190	55.2	60	600	440	1.14	2.60	~ 0.14[+]	0.30	8.3	23.06	22.18	Off $(\bar{1}\bar{1}\bar{1})$B
12137	200	60	60	600	440	1.05	3.05	~ 0.12[+]	0.26	10.0	27.78	24.43	Off $(\bar{1}\bar{1}\bar{1})$B
12167	184	51.7	60	600	450	0	2.60	0	0	10.0	27.78	38.42	$(\bar{1}\bar{1}\bar{1})$B
12197	172	34.2	60	600	440	0	1.18	0	0	5.0	13.89	42.24	$(\bar{1}\bar{1}\bar{1})$B
1078	172	27.2	90	600	460	0	1.47	0	0	10.0	18.52	45.43	Off $(\bar{1}\bar{1}\bar{1})$B
1098	164	32.4	60	600	440	0	1.09	0	0	4.0	11.11	38.81	Off $(\bar{1}\bar{1}\bar{1})$B
1118	170	39.9	35	600	440	0	---	0	0	A	A	A	Off $(\bar{1}\bar{1}\bar{1})$B

[+] = No X-ray data available, estimated from EDAX.
A = Aborted run.

(3) $(\bar{1}\bar{1}\bar{1})$ As face etched for 15 minutes in 4:1:1 $H_2SO_4/H_2O_2/H_2O$ followed by a 1 minute 2 percent $Br:CH_3OH$ etch (Films 9017 through 9077).

(4) 14° off - $(\bar{1}\bar{1}\bar{1})$ As face etched as in (3) (Films 9097 through 9297).

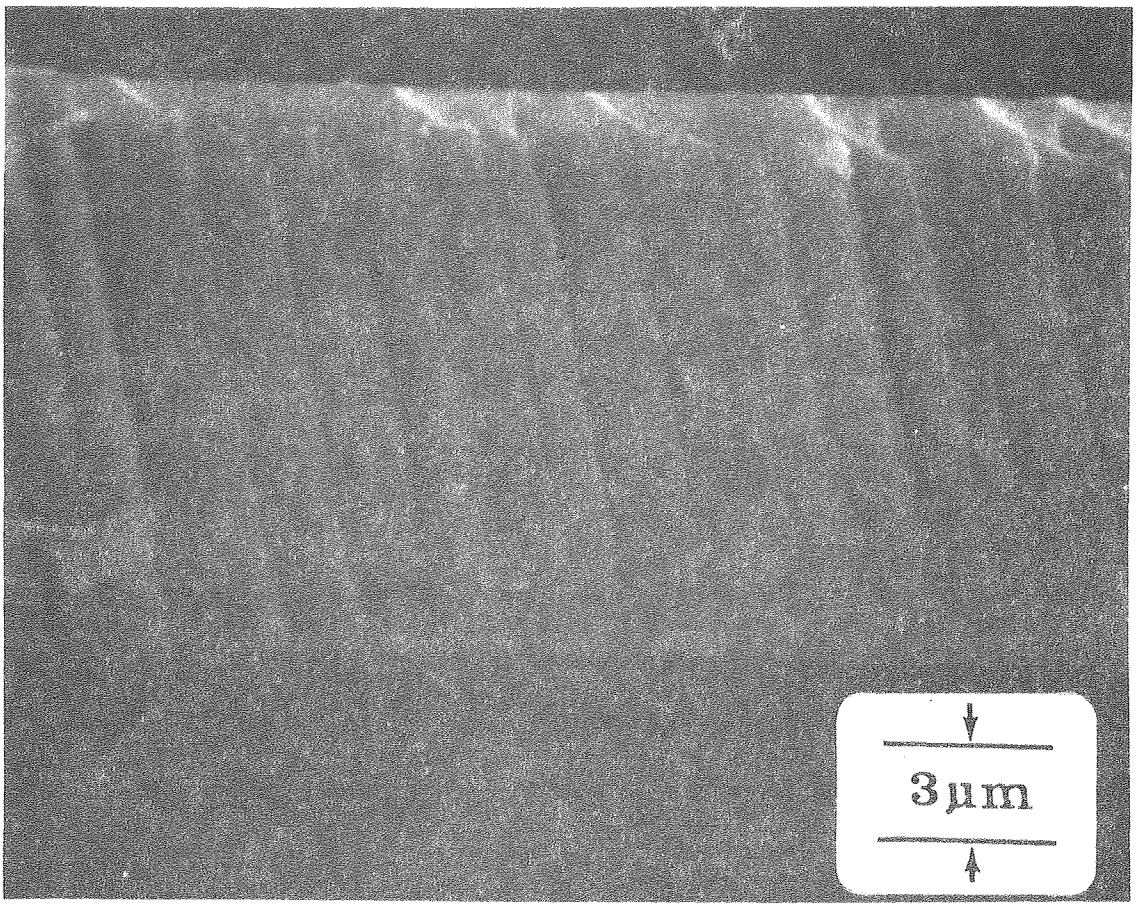
All GaAs deposition surfaces were initially mechanically polished with 1μ and 1/4 μ diamond grit before etching. Prior to placement in the vacuum system all substrates were washed in CH_3OH and then blown dry with N_2.

All (Cd,Zn)S single crystal films grown on the (111) Ga face were cracked regardless of the etchant. It was believed that a thin film of GaS formed between the GaAs and the growing film. X-ray and electron diffraction, and EDAX analysis confirmed the presence of this sulfide. This film could be formed during the substrate preheating procedure or in the early stages of the deposition. There is some evidence in the literature to support this interpretation of our results: Auger electron and x-ray photoemission spectroscopy have shown there is an excess of Ga after a $Br:CH_3OH$ etch of the GaAs surface.[10] Weinstein and Wolff[11] determined that for CVD epitaxial growth of CdS on the (111) Ga-face of GaAs the S-atom always attached first to the substrate surface. This allows minimization of the electrostatic interfacial energy.[12] Therefore, with the (111) Ga-face substrates used in the present study the Ga-rich surface layers after etching may incorporate sulfur leading to the formation of a GaS layer which does not form with CVD because of in situ

substrate etching. To prevent cracking of the mixed crystal film the $(\bar{1}\bar{1}\bar{1})$ As face was used as the deposition surface. Since, on this face, the first incorporated species is the cation, and etching does not leave a gallium excess; there is no GaS formation, and the films were uncracked.

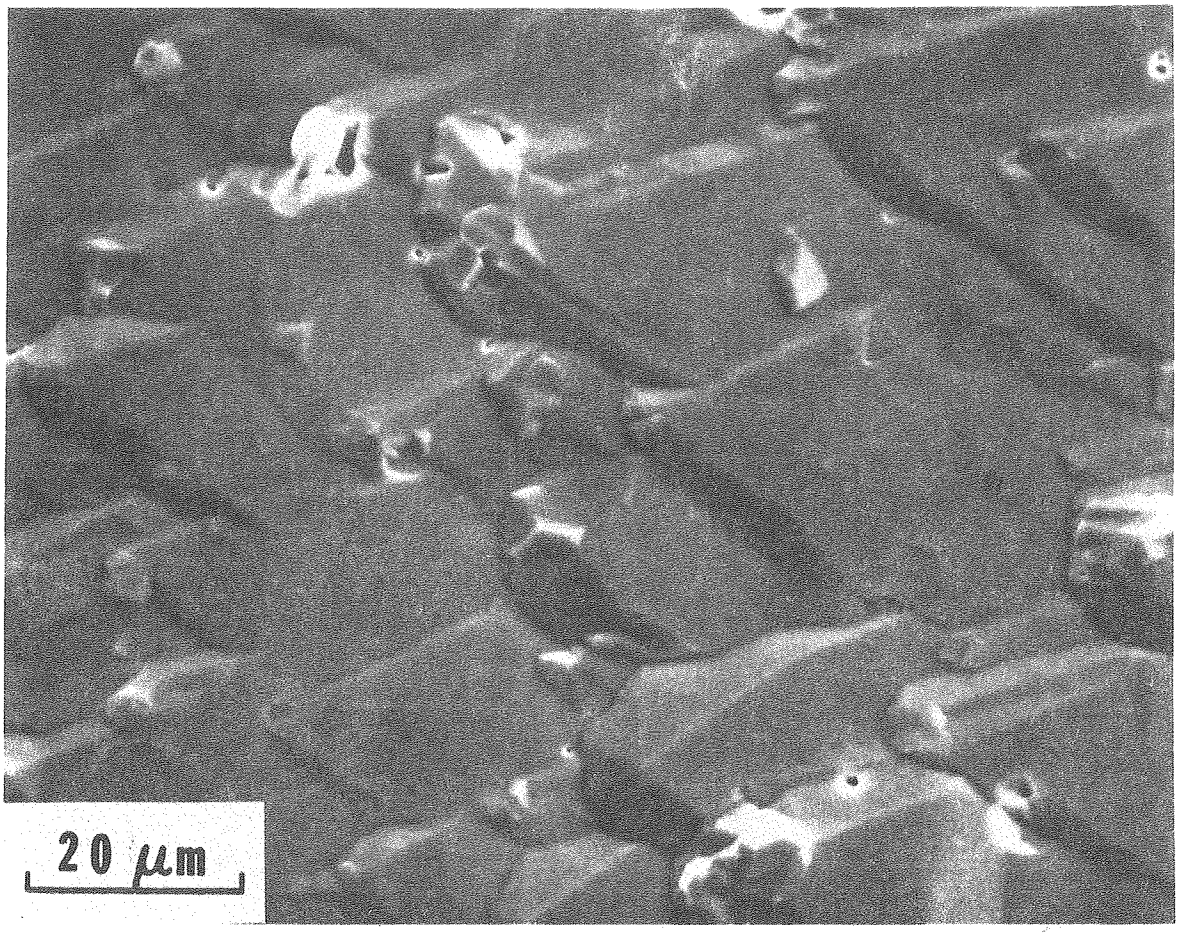
Crack-free films have also been produced on substrates tilted 14° away from $(\bar{1}\bar{1}\bar{1})$. An interesting feature of film growth on these tilted substrates is that they do not show as dramatic a dependence of composition on the relative source evaporation rates as do the exact (111) substrates. The extreme sensitivity of film composition to deposition parameters for (111) substrates was discussed in the previous section. Furthermore, as might be expected for higher step-density substrates, the growth rates were higher with the tilted substrates. However, it was observed that many of the films deposited on the As face showed polycrystalline growth which may have been a result of the higher growth rates.

Figures 3.15 through 3.17 show SEM micrographs of films grown on tilted substrates. Figure 3.15 shows the cleaved edge of a film where the cleavage steps are seen to be parallel to the substrate <111> direction, just as in the case of non-tilted (111) substrates. In Fig. 3.16 (Film 9207) elongated hexagonal faces are seen on the top surface. A markedly different surface morphology showing ledges is seen in Fig. 3.17 (Film 9107) in which the normalized growth rate was lower. These ledges were perpendicular to the axis of rotation away from the (111) substrate plane.



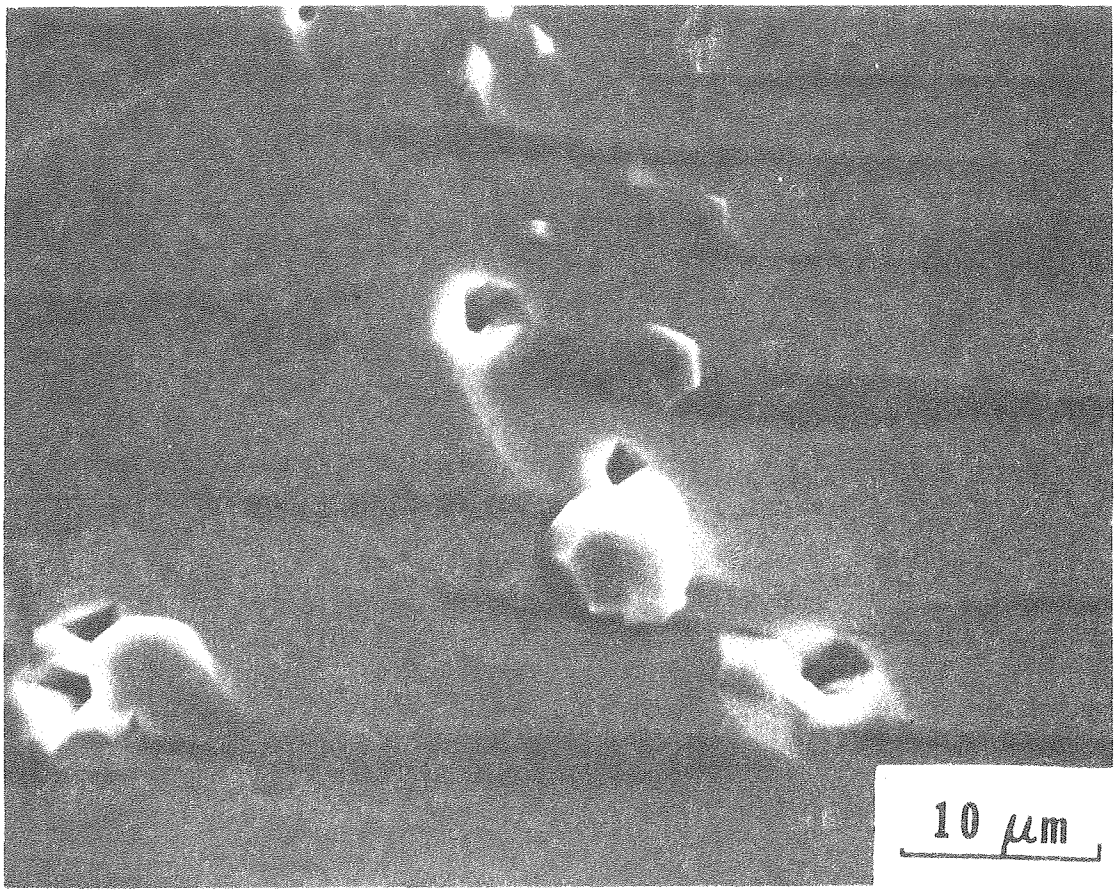
XBB 779-9107

Figure 3.15



XBB 779-9474

Figure 3.16



XBB 779-9106

Figure 3.17

To eliminate the possibility of further variations in substrate surface condition, sputter-etching equipment was installed. Also to obtain a cleaner vacuum (mainly reduction in hydrocarbons present) a turbomolecular pump (Leybold-Heraeus 450 Turbovac) was used to replace the oil diffusion pump. Experiments using the sputter-etch procedure (Films 12067 through 1118) were conducted on the following two GaAs surfaces:

(1) ~14°-off $(\bar{1}\bar{1}\bar{1})$ As face

(2) Cr-doped $(\bar{1}\bar{1}\bar{1})$ As face with $\rho > 10^6$ Ω-cm

The latter substrates were to be used in making measurements of the film resistivity. Both sets of substrates were given the following etch procedure due to A. H. Kachare[13]

(1) 5 mins. 3:1 :: H_2SO_4:H_2O

(2) 1 min. 5:1:1 :: H_2SO_4:H_2O_2:H_2O

(3) 1 min. 7:1 :: H_2SO_4:H_2O (immediately preceding deposition)

All solutions were cooled in an ice bath. The substrates were washed in methyl alcohol and blown dry with N_2 prior to placement in the vacuum system.

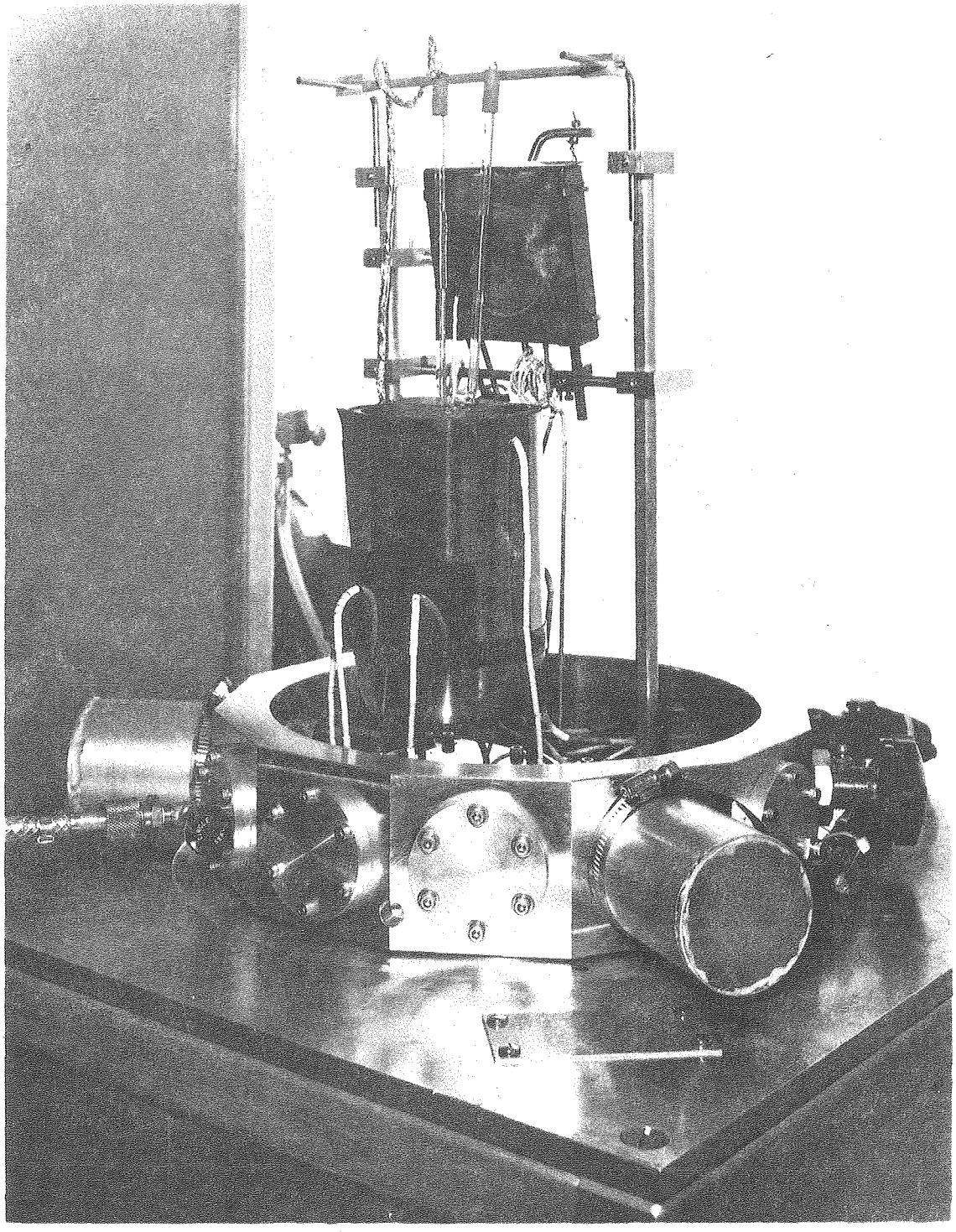
In operation, to begin the sputter etching, argon was leaked into the chamber while the main gate valve was throttled so that the pressure was approximately 150 millitorr. D.C. voltages between 500 V and 2.6 kV were used for times of 2-10 minutes with a cathode-anode distance of approximately 2.5 cm. The substrate and cylinder were then heated and the usual deposition procedure initiated. A

photograph of the deposition apparatus with sputter-etch facilities is shown in Fig. 3.18.

Lower growth rates, between 11-30 Å/sec, were used for both kinds of substrates. All films grown on sputter-etched substrates had both (002) and off c-axis diffraction peaks as found by x-ray diffraction. Single crystal and polycrystalline regions on the same film were observed in the SEM as shown in Fig. 3.19. A summary of film growth experiments using the sputter-etch procedure is given in Table 3.4A.

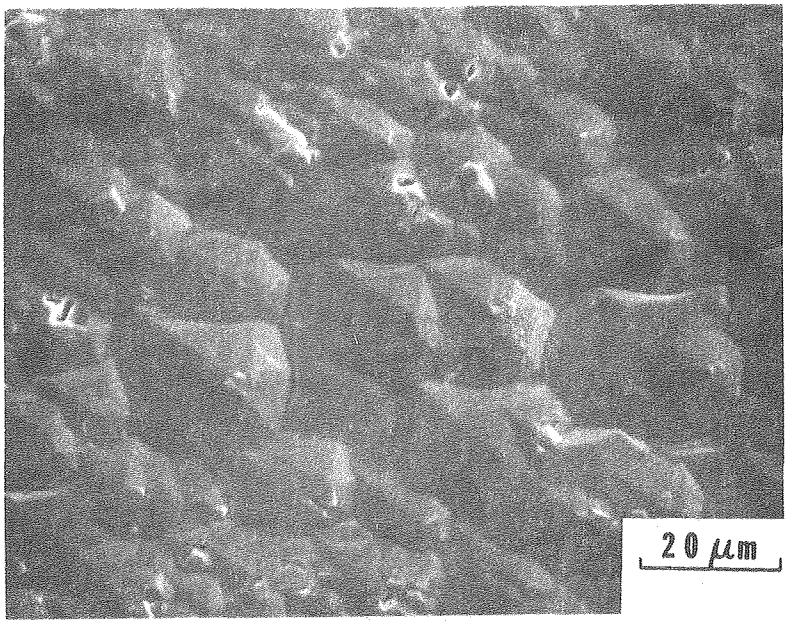
A possible explanation for the polycrystalline growth is extensive ion damage to the substrate surface from the sputter-etch procedure which would create heterogeneous nucleation sites. Figure 3.20 shows the growth of randomly oriented CdS grains from the shortened deposition Run 1118. Films 1138 and 1178 were deposited under the same conditions as the previous three runs but without the sputter-etch procedure. The improved epitaxy resulting in a highly specular surface is shown in Fig. 3.21.

Since growth on Ga face GaAs substrates was found to be greater than on the As face and epitaxy more readily achieved deposition Runs 1208 through 3098 were grown on 14°-off (111) Ga face substrates (see Table 3.4B). Some (Cd,Zn)S films were too thin (<1 μm) for analysis as can be seen in Table 3.4B. This was due to the very sensitive dependence of growth rate on the relative evaporation rates of CdS and ZnS, as discussed in the previous section.

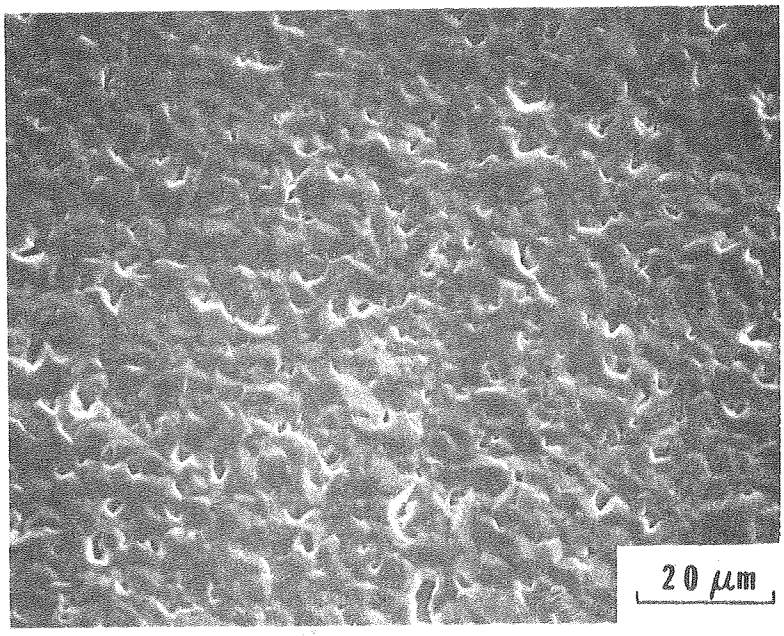


CBB 781-460

Figure 3.18



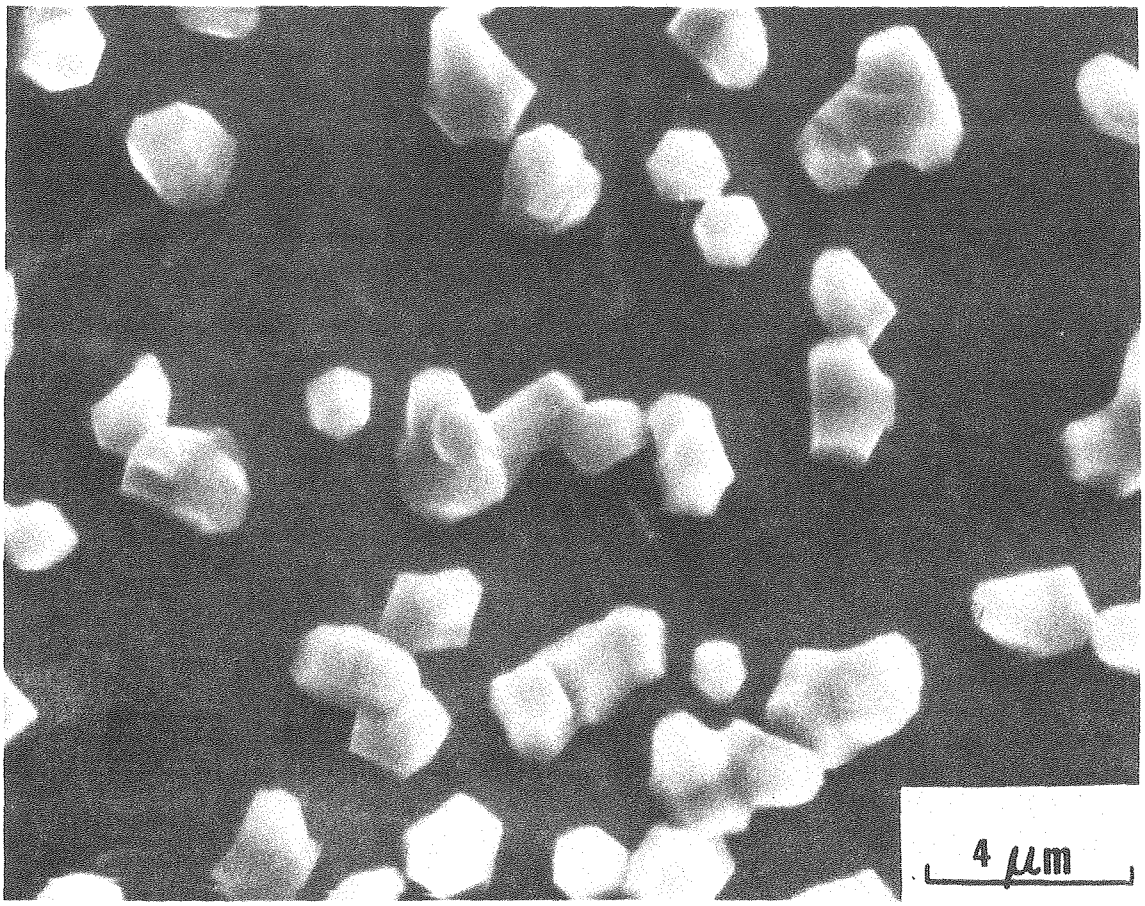
a



b

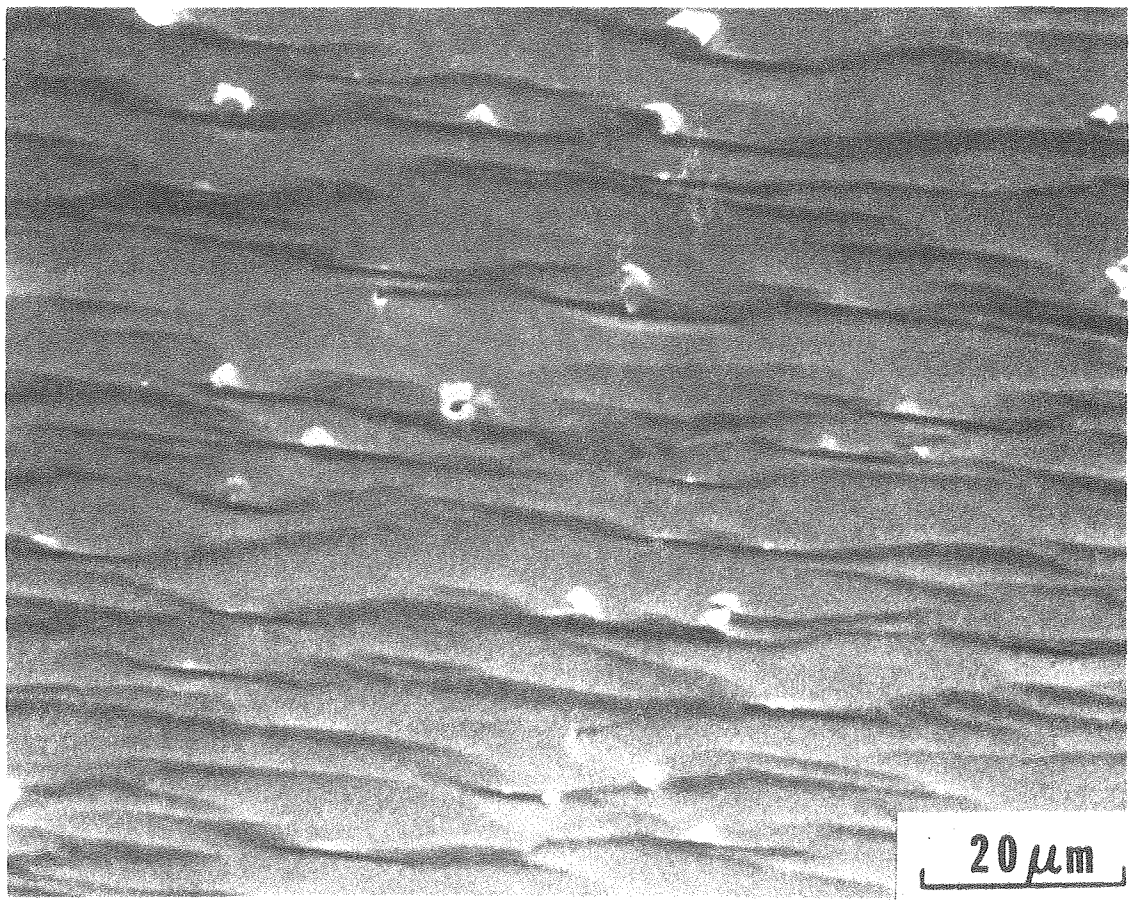
XBB 781-573

Figure 3.19



XBB 784-4137

Figure 3.20



XBB 784-4138

Figure 3.21

Table 3.4B. Effect of GaAs Substrate Preparation and Orientation

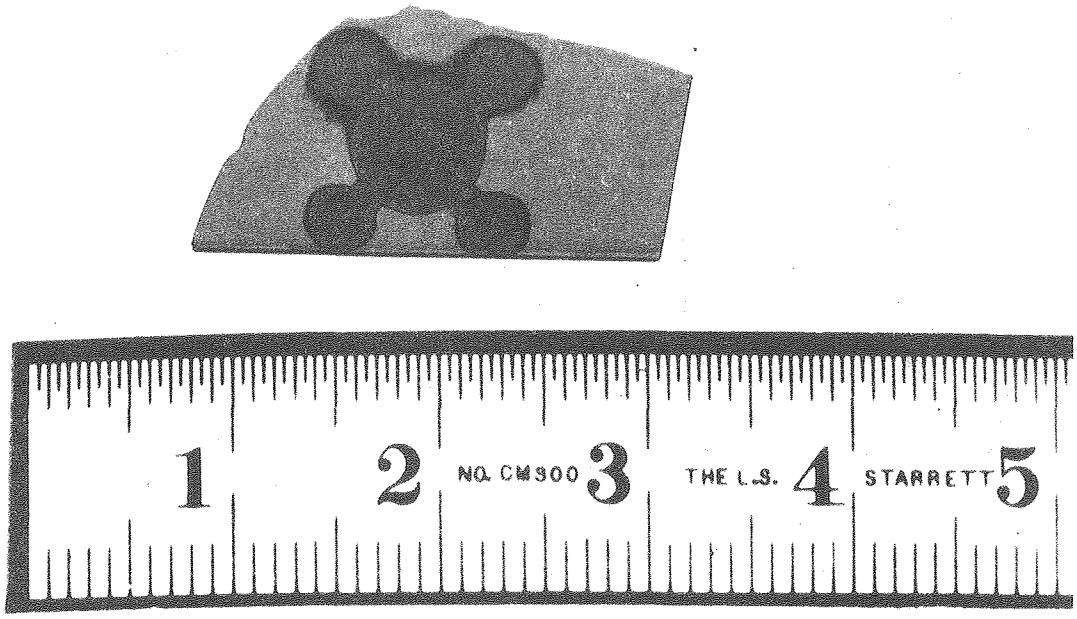
Run	ZnS Power (watts)	CdS Power (watts)	Run Duration (minutes)	Cylinder Temp. (°C)	Substrate Temp. (°C)	ZnS Rate R_{ZnS} (mmole/hr)	CdS Rate R_{CdS} (mmole/hr)	ZnS Mole Fraction	Θ ((R_{ZnS}/R_{Total}))	Thickness τ (μm)	$d\tau/dt$ (Å/sec)	Growth Rate g (Å/μmole)	Substrate
1138	184	39	60	600	490	0	1.22	0	0	6.0	16.67	49.25	Off $(\bar{1}\bar{1}\bar{1})$B
1178	175	41	60	600	520	0	1.32	0	0	6.0	16.67	45.38	Off $(\bar{1}\bar{1}\bar{1})$B
1208	188	38	60	600	500	0	1.68	0	0	15.0	41.67	89.54	Off (111)A
1248	192	38	60	600	500	1.10	1.59	0.23	0.41	9.0	25.00	33.54	Off (111)A
1278	204	40	60	600	500	0	1.76	0	0	15.0	41.67	85.31	Off (111)A
1308	126	32	60	600	525	0	0.71	0	0	9.0	25.00	127.47	Off (111)A
2028	152	33	60	600	560	0.43	1.21	0.03	0.26	12.3	34.17	74.89	Off (111)A
2078	158	34.2	60	600	550	0.37	0.84	0.15	0.31	10.6	29.44	87.82	Off (111)A
2098	164	32.4	60	600	530	0.28	0.98	0.03	0.22	11.3	31.47	90.41	Off (111)A
2278	137	30	60	600	420	0	0.32	0	0	3.0	8.33	94.22	Off (111)A
2288	122	30	60	600	460	0.12	0.35	*	0.26	*	*	*	Off (111)A
3028	136	40	60	600	490	0.15	0.62	*	0.20	*	*	*	Off (111)A
3088	134	40	60	600	480	0.08	0.66	0.03	0.11	5.5	15.28	74.35	Off (111)A
3098	136	42	65	600	480	0.09	0.75	*	0.11	*	*	*	Off (111)A
5268	118	38	60	600	490	0	0.57	0	0	*	*	*	$(\bar{1}\bar{1}\bar{1})$As
5308	140	36	60	600	470	0	0.42	0	0	*	*	*	$(\bar{1}\bar{1}\bar{1})$As
6028	130	44	60	600	480	0	0.64	0	0	*	*	*	$(\bar{1}\bar{1}\bar{1})$As
6068	140	44	60	600	480	0	0.69	0	0	2.0	5.56	28.9	(111)Ga
6088	130	55	60	600	485	0	0.87	0	0	2.4	6.67	27.5	(111)Ga
8298	152	74	120	600	480	0	1.03	0	0	6.5	9.03	31.5	(111)Ga
8308	216	93	120	600	420	0.85	1.58	0.08	0.35	8.0	11.11	16.5	(111)Ga
8318	261	93	120	600	420	1.62	0	1.00	1.00	*	*	*	(111)Ga
9078	161	48	60	600	430	0	0.81	0	0	3.5	9.72	43.2	(111)Ga

* = Film thickness less than 1 μm; difficult to analyze.

d. Films Grown in Van der Pauw Geometry

In order to correlate the structural perfection of the grown films with their electrical properties, Hall Effect experiments were performed to determine values for carrier concentration and mobility. CdS films in the Van der Pauw geometry[14] (see Fig. 3.22) were deposited onto insulating ($\rho > 10^7$ Ω-cm, chromium doped) (111) and 12°-off (111) towards (110) GaAs substrates. It was found that CdS films grown on the As face were polycrystalline whereas films grown on the Ga face were single crystal. An order of magnitude difference in Hall mobility was found for these samples as discussed in Section 5.1.

Yoshikawa and Sakai[15] reported that CdS films grown on GaAs substrates in H_2 gas by the close-spaced technique resulted in films with low resistivity and carrier concentration as high as 5×10^{19} cm^{-3}. They determined for films grown at substrate temperatures of 750°C for 10 min. that the dominant donor species was Ga which had diffused from the GaAs substrate. CdS films for Hall Effect measurements were grown on quartz and Corning 7059 substrates to investigate the effects of autodoping. It was found, however, that all films grown on these substrates were non-adherent even after altering several processing parameters and substrate preparation techniques. Our Hall measurements made on single crystal and polycrystalline films grown on GaAs substrates are discussed in Section 5.1. The results for films grown in the Van der Pauw geometry for Hall Effect measurements are summarized in Table 3.5.



CBB 783-2708

Figure 3.22

Table 3.5. Films Grown in Van der Pauw Geometry

Run	ZnS Power (watts)	CdS Power (watts)	Run Duration (minutes)	Cylinder Temp. (°C)	Substrate Temp. (°C)	ZnS Rate R_{ZnS} (mmole/hr)	CdS Rate R_{CdS} (mmole/hr)	ZnS Mole Fraction	Θ (R_{ZnS}/R_{CdS})	Substrate
2148	113	34.2	60	600	480	0	0.34	0	0	(111)Ga
2158	136	33	60	600	420	0.10	0.37	*	0.22	(111)Ga
6148	130	70	60	600	465	0	1.29	0	0	$(\bar{1}\bar{1}\bar{1})$As
6158	126	60	90	600	480	0	1.25	0	0	$(\bar{1}\bar{1}\bar{1})$As
6198	122	53	90	600	460	0	1.22	0	0	Off (111)Ga
6208	122	59	60	600	470	0	0.79	0	0	Off (111)Ga
6218	133	57	120	600	460	0	0.64	0	0	$(\bar{1}\bar{1}\bar{1})$As
7258	119	57	60	600	470	0	0.87	0	0	Quartz
7268	135	70	60	600	460	0	1.40	0	0	Quartz
7278	137	70	60	600	470	0.13	1.25	0.03	0.10	Quartz
8018	145	73	60	600	440	0.13	1.20	0.03	0.10	Quartz
8148	164	74	60	600	440	0	1.29	0	0	Corning 7059
8168	148	81	60	600	420	0	1.47	0	0	Corning 7059
8178	202	73	60	600	450	0	1.37	0	0	Corning 7059
8288	130	70	120	500	350	0	—	0	0	Corning 7059

* = Film thickness less than 1 μm; difficult to analyze.

e. Films Grown on (111) Ge Substrates

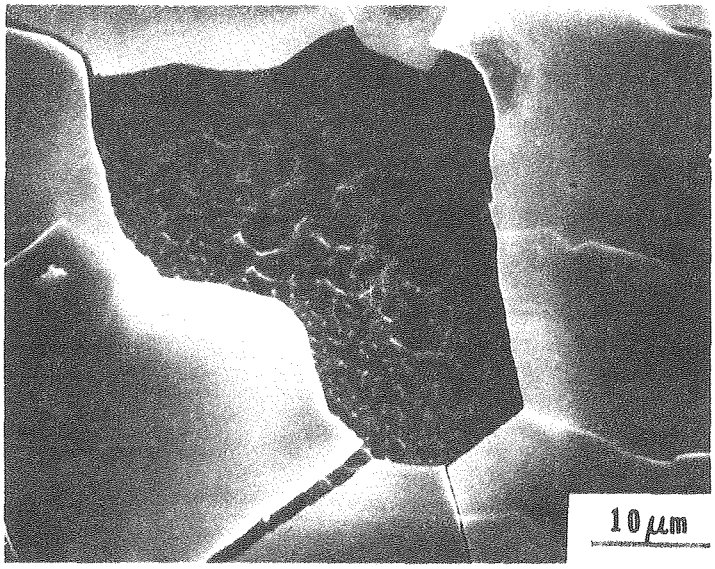
Single crystal CdS and (Cd,Zn)S films were grown on GaAs substrates because of the good thermal expansion and lattice parameter match. However, current-voltage measurements of the n-CdS/n-GaAs heterojunction showed a non-ohmic characteristic. Efforts were made to etch the GaAs from the grown single crystal film for backwall cell construction, but the thickness of the films (usually less than 10 μm) made handling extremely difficult (see the results for films grown on GaAs substrates in Tables 3.4A and 3.4B).

To facilitate front-wall cell construction, a semiconductor substrate forming an ohmic back contact was sought. Growth experiments were conducted on (111) n-Ge substrates because of the good thermal expansion and lattice parameter matching and its larger electron affinity than GaAs (see Table 3.1). CdS and (Cd,Zn)S films were deposited on Ge substrates (purchased from Eagle-Picher, $\rho \sim 5$ Ω-cm) under growth conditions similar to those for GaAs substrates. These films, however, were non-adherent. Abdalla, Holt and Wilcox[16] observed no CdS film growth on Ge substrates heated above 550°C which they attributed to sulfur attack of the Ge resulting in a pitted surface. Epitaxial CdS films were grown on Ge by lowering the substrate temperature to approximately 320°C at the beginning of the deposition. Good quality single crystal films of CdS were grown at the lower substrate temperatures but upon addition of Zn, the (Cd,Zn)S and further CdS films were cracked as shown in Fig. 3.23. In some cases the films cracked during growth and etching of the Ge

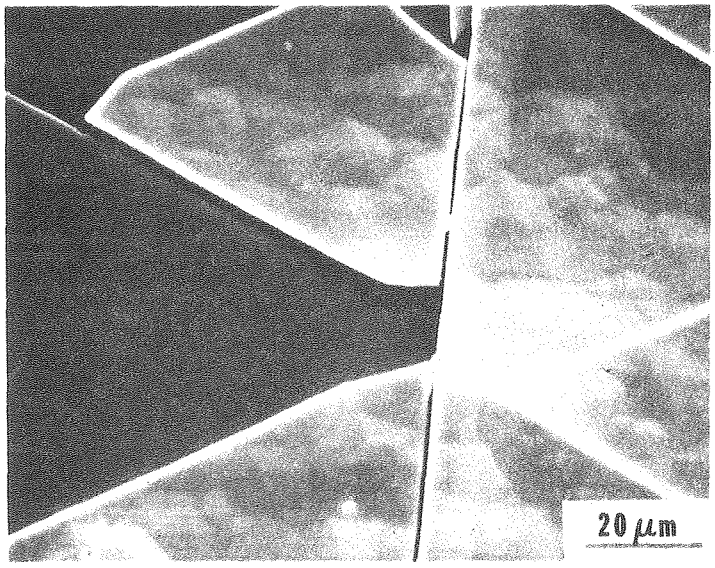
occurred through the cracks (Fig. 3.23a) resulting in non-adherent films. These growth results are summarized in Table 3.6A.

Since cracking only occurred after a ZnS evaporation, it was believed that the exclusion of Zn from the growth chamber would eliminate this problem. An extensive cleaning and out-gassing procedure was conducted before each growth run. Uncracked single crystal CdS films were then routinely deposited. (Cd,Zn)S films were grown by initially depositing a CdS layer (see Table 3.6B). Because the hot-wall cylinder was cleaned before each growth run, the effect of cylinder wall temperature on growth rate could be more accurately determined as shown in Fig. 3.24.

An effect of supersaturation on surface morphology was also observed. Figure 3.25a shows the top surface of a single crystal CdS film grown on (111) Ge in which the surface morphology is dominated by hexagonal pyramids. Christmann, Jones and Olsen (CJO)[17] found for CdS grown epitaxially on SrF_2 substrates that the hexagonal pyramids were associated with an excess amount of cadmium, and that they could be formed by growth around a cadmium droplet. Cadmium droplets formed when conditions existed which did not allow the cadmium adatoms sufficient time to diffuse to their equilibrium positions. Figure 3.25b is a SEM micrograph of a single crystal CdS film grown at a lower cylinder temperature in which the supersaturation was less than in the previous example. Hexagonal flat-tops are dominant which is in agreement with CJO who showed that this morphology was the equilibrium growth form produced by two-dimensional nucleation.



a



b

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Figure 3.23

Table 3.6A. Film Growth Experiments on (111)Ge Substrates

Run	ZnS Power (watts)	CdS Power (watts)	Run Duration (minutes)	Cylinder Temp. (°C)	Substrate Temp. (°C)	ZnS Rate R_{ZnS} (mmole/hr)	CdS Rate R_{CdS} (mmole/hr)	ZnS Mole Fraction	Θ (R_{ZnS}/R_{Total})	Thickness τ (μm)	$d\tau/dt$ (Å/sec)	Growth Rate, g (Å/μmole)
9148	157	50	60	600	420 → 450	0	---	0	0	NA	NA	NA
9158	144	60	60	600	400 → 440	0	0.66	0	0	NA	NA	NA
9198	165	52	60	600	415 → 450	0.13	0.66	---	0.17	NA	NA	NA
9218	154	51	60	540	320 → 420	0	0.17	0	0	*	*	*
9228	158	65	90	530	300 → 420	0	0.24	0	0	*	*	*
9258	190	73	60	520	300 → 410	0.18	0.71	0.08	0.21	1.0	2.78	11.1
9298	192	84	120	520	315 → 410	0.17	0.81	0.08	0.18	2.5	3.47	12.7
10038	184	84	60	520	320 → 400	0.15	0.72	0.16	0.18	1.0	2.78	11.4
11038	184	84	60	560	320 → 420	0	1.80	0	0	3.9	10.83	21.7
11078	264	99	60	570	320 → 430	1.10	1.58	0.27	0.41	3.0	8.33	11.2
11088	239	97	60	545	330 → 400	0.45	1.09	0.20	0.29	2.0	5.56	13.0
11218	209	96	120	520	290 → 360	0.09	0.63	LS1	LS1	1.0	LS1	LS1
11288	255	96	150	510	310 → 390	0.42	0.64	LS1	LS1	*	LS1	LS1
11298	255	96	180	500	320 → 375	0.44	1.27	LS1	LS1	4.2	LS1	LS1
12058	258	96	180	510	320 → 350	0.88	0.75	LS1	LS1	4.2	LS1	LS1
12158	220	96	120	500	300 → 380[SS]	0.28	0.76	---	0.27	NA	NA	NA
1159	220	96	120	500	300 → 390[SS]	0.31	0.97	---	0.24	NA	NA	NA

NA = Non-adherent film
* = Film thickness less than 1 μm, difficult to analyze
LS1 = Layer Structure 1: (Cd,Zn)S/ZnS/Ge
SS = Stainless steel substrate holder used

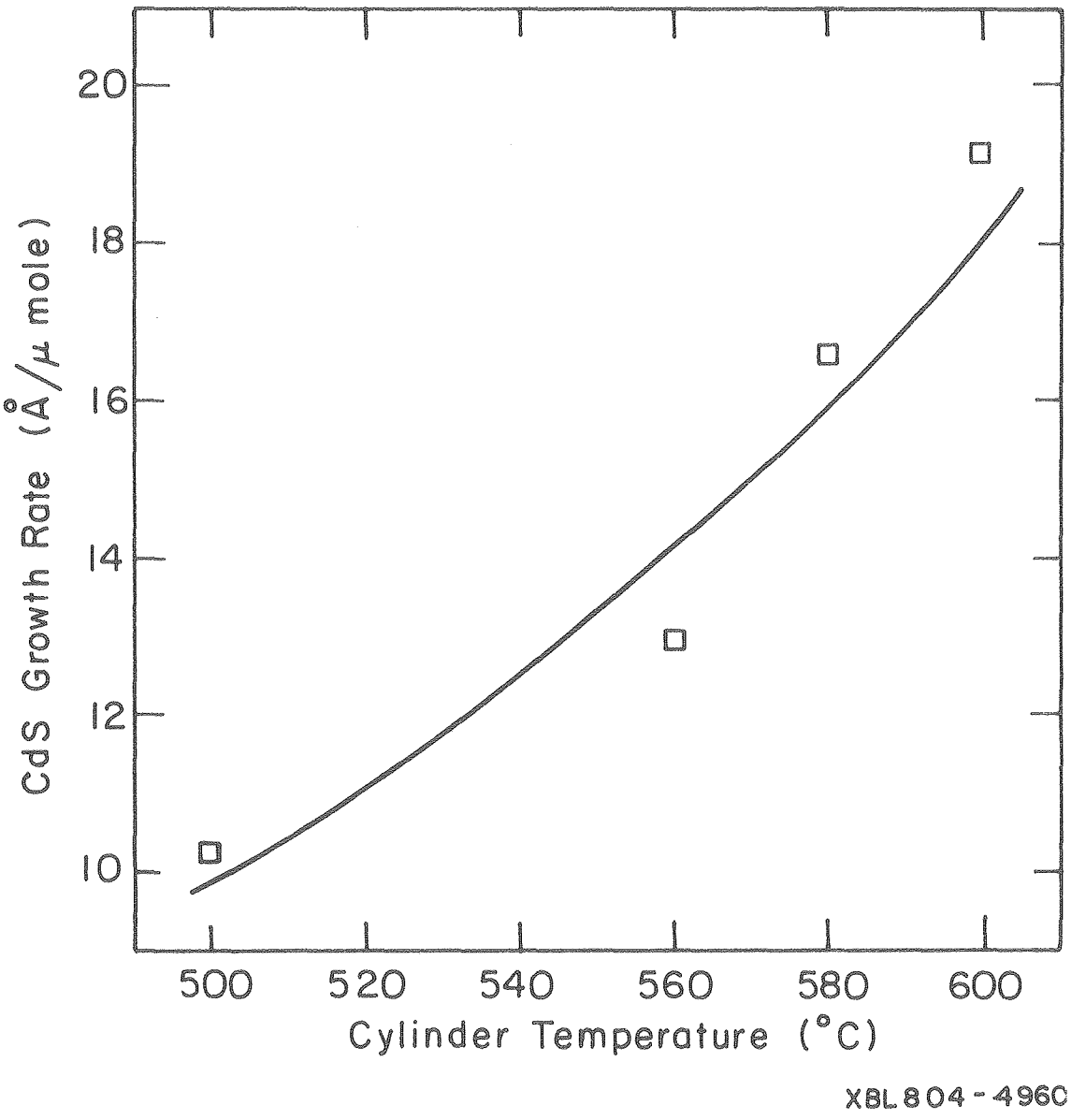
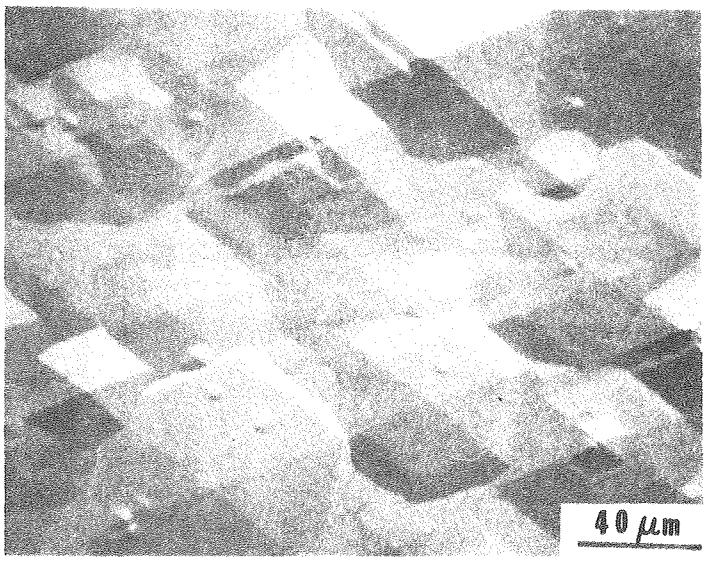

CdS Growth Rate (Å/μ mole)
20
18
16
14
12
10
500
520
540
560
580
600
Cylinder Temperature (°C)
XBL 804-4960

Figure 3.24

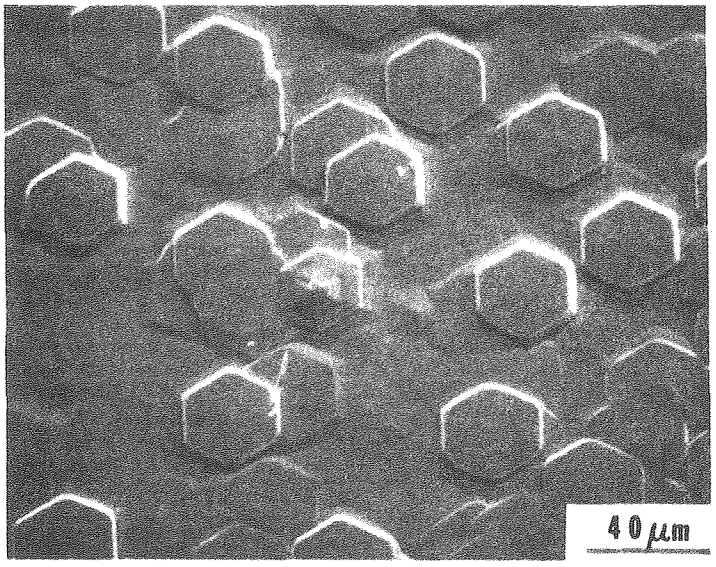
Table 3.6B. Film Growth Experiments on (111)Ge Substrates Using Outgassing Procedure

Run	ZnS Power (watts)	CdS Power (watts)	Run Duration (minutes)	Cylinder Temp. (°C)	Substrate Temp. (°C)	ZnS Rate R_{ZnS} (mmole/hr)	CdS Rate R_{CdS} (mmole/hr)	ZnS Mole Fraction	Θ (R_{ZnS}/R_{Total})	Thickness τ (μm)	$d\tau/dt$ (Å/sec)	Growth Rate, g (Å/μmole)
4209	108	124	180	500	300 → 400	0	1.30	0	0	4.0	3.70	10.3
4249	111	122	210	560	320 → 450	0	2.66	0	0	12.0	9.52	12.9
5019	114	109	180	600	330 → 450	0	1.75	0	0	10.0	9.26	19.1
5179	128	93	150	580	335 → 450	0.06	1.02	~ 0	0.06	4.0	4.44	14.8
5239	240	111	120	600	340 → 500	1.57	3.74	0.21	0.30	15.0	20.83	14.1
5309	190	92	150	580	320 → 460	0.49	2.30	0.17	0.18	10.0	11.11	14.3
6269	244	118	180	580	340 → 480	1.02	1.80	LS2	LS2	14.0	LS2	LS2
8249	105	120	180	580	330 → 390	0	2.05	0	0	8.0	7.41	13.0
8319	270	63	180	550	340 → 490	1.26	1.33	LS3	LS3	2.9	LS3	LS3
9269	105	120	180	530	320 → 400.	0	1.68	0	0	1.7	1.57	3.4
1040	100	108	180	580	320 → 360	0	1.21	0	0	6.0	5.56	16.6

LS2 = Layer Structure 2: $(Cd_{0.83}Zn_{0.17})S/CdS/Ge$
LS3 = Layer Structure 3: ZnS/CdS/Ge



a



b

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Figure 3.25

4. Transmission Electron Microscopy Studies

4.1 Single Crystals

The microstructure of a typical single crystal CdS film grown at this laboratory is shown in the electron micrographs in Figs. 4.1a, b and c. A loose network of curved dislocation lines along non-crystallographic directions as in Fig. 4.1a is most commonly observed. The dislocations lie mainly in the plane of the foil, i.e., in the basal plane of the hexagonal wurtzite structure of CdS. However, structures as in Figs. 4.1b and c are also found in the same film with many of the dislocations lying at an angle to the basal plane and hence intersecting the foil surfaces. The dislocation density in Fig. 4.1c corresponds to that of a well-annealed film of CdS as shown by Wilcox and Holt,[18] while Figs. 4.1a and b have somewhat higher densities.

No evidence of either the cubic form of CdS (sphalerite structure), twins, or of planar faults (e.g., stacking faults or anti-phase boundaries) was found in any of the CdS films grown on (111) Ge substrates. This is in agreement with the literature which reports observing such planar faults or cubic inclusions only for the growth of CdS on other substrates and surface orientations.[16,18] Also in accord with the literature,[18] dislocation loops were observed as shown by the arrows in Fig. 4.1. The nature and origin of these loops have not yet been determined. More generally there are no published experimental results on the nature of dislocations in CdS and their Burgers vectors. This severe lack of experimental data on such

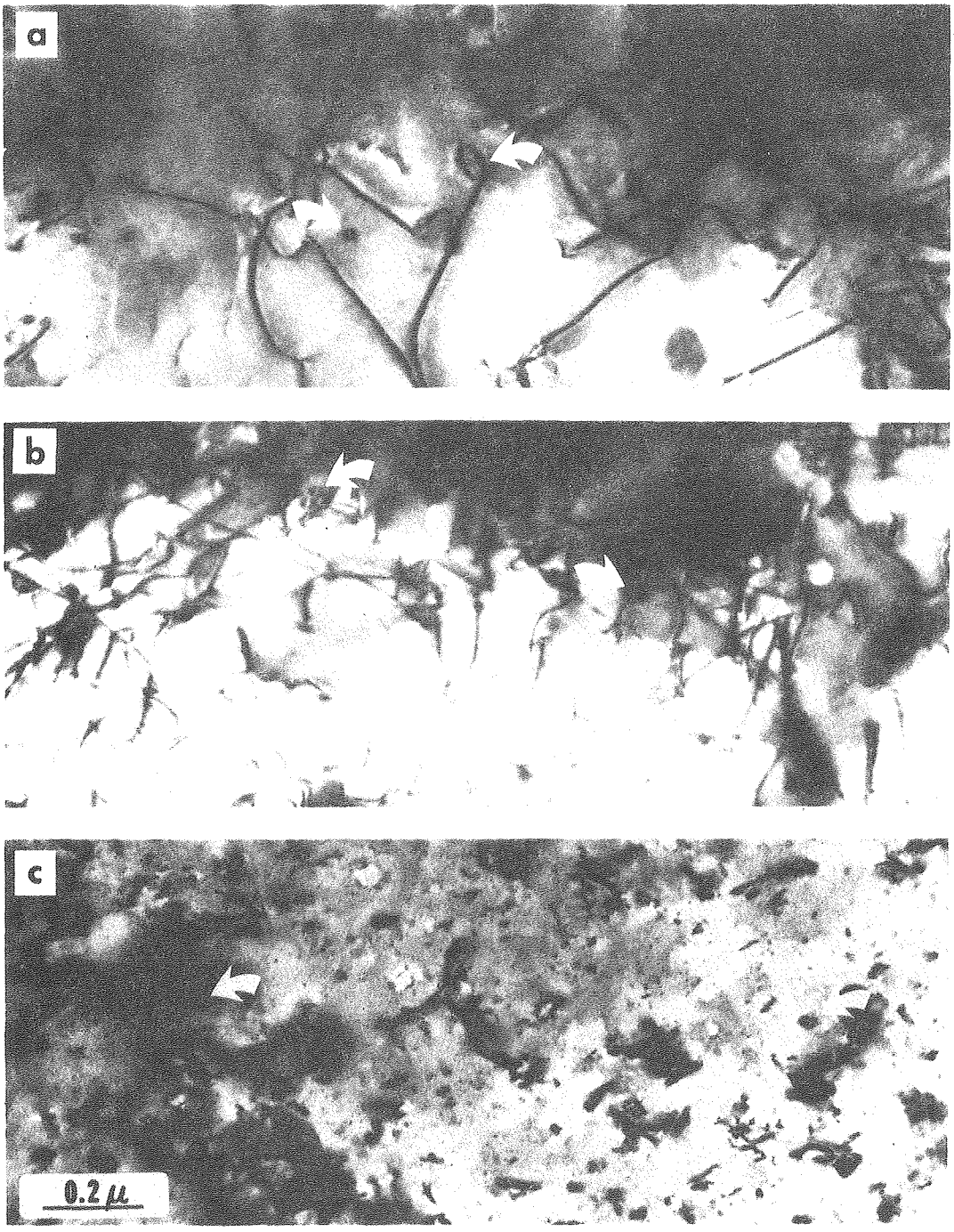

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Figure 4.1

elementary defects in CdS must be attributed to the extreme difficulty of preparing thin foils for electron microscopy from "thick" (~ 10 μm) films. (One way to circumvent this problem is, of course, to grow very thin films (< 1 μm), but such films might not be representative of the thicker films actually used in devices.)

Because of the difficulties in thinning foils for electron microscopy, a more detailed account of the technique used is given in Section 4.3. Fig. 4.1 is representative of the quality of foils prepared by the most successful technique perfected only recently. All other electron micrographs in this report contain artifacts which are attributed to the thinning procedure. Some of them are severe enough to mask entirely the original microstructure of the film.

The spotty background structure in Fig. 4.2 is one of the minor artifacts encountered and is weak enough still to allow a partial dislocation analysis. Figs. 4.2a, b and c are electron micrographs of the same area in a single crystal CdS film, using different diffracting conditions ($\bar{g}$-vectors). If the Burgers vector $\bar{b}$ of a dislocation is perpendicular to the $\bar{g}$-vector in a given diffracting condition, the dislocation will be invisible ($\bar{g}\cdot\bar{b} = 0$). This is shown in Fig. 4.2 for the dislocations near x and y. In Fig. 4.2c both dislocation lines are visible. In addition to the dislocation from x to y, there is apparently another dislocation which is parallel to the first one at x and is bent at its ends. These two dislocations are separately out of contrast in Figs. 4.2a and b, respectively showing that they have different Burgers vectors; one with a component

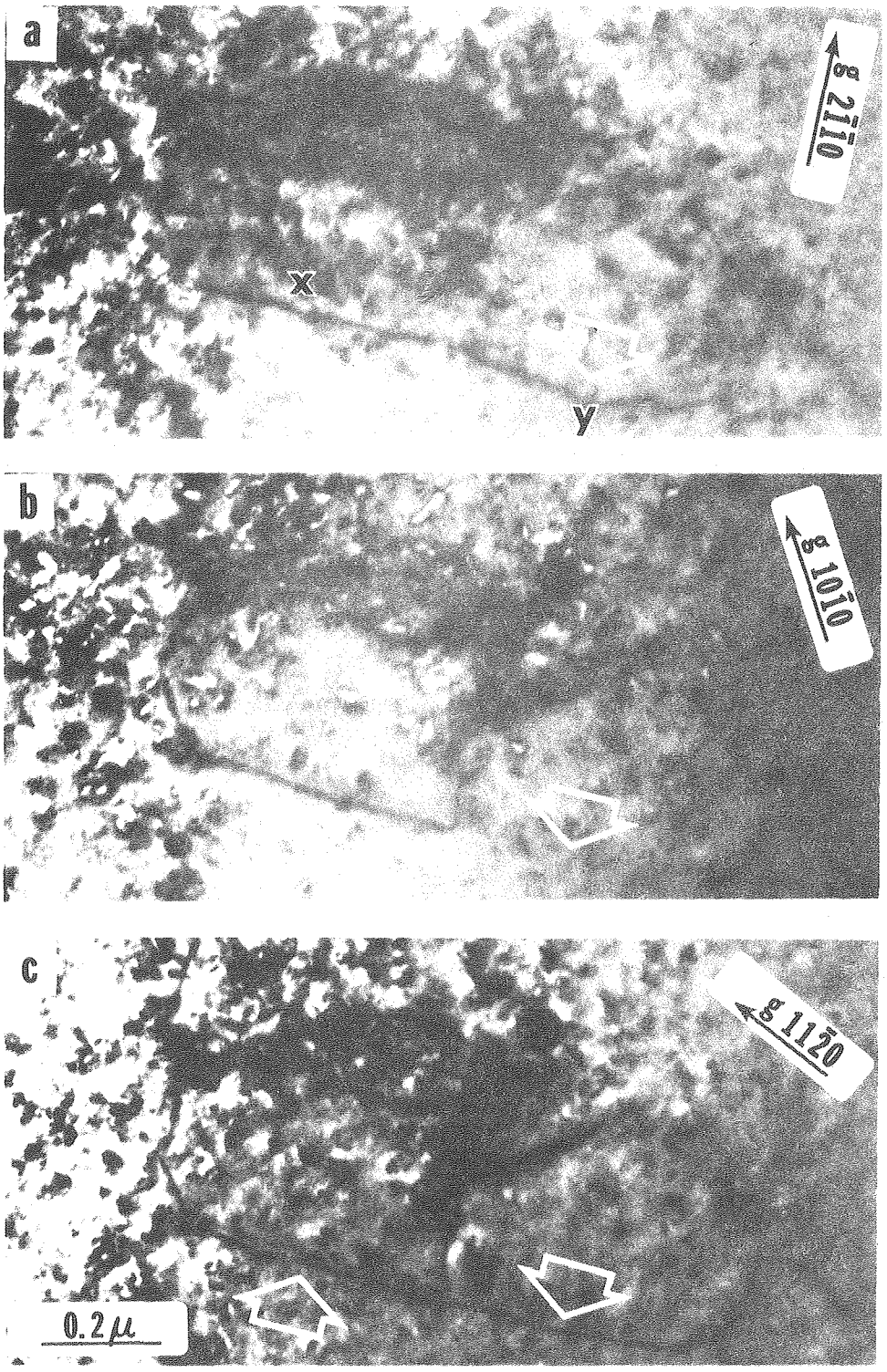

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Figure 4.2

along $[01\bar{1}0]$ and the other one with a component along $[1\bar{2}10]$. A more complete analysis must also establish the components of the Burgers vectors along the c-axis (if any), i.e., at least two diffracting conditions for which $\bar{g}\cdot\bar{b} = 0$ must be found. The analysis presented in Figs. 4.1 and 4.2 is an example of the type of TEM work anticipated for future studies on CdS films which are now possible because of the development of a successful thinning technique. Similar electron microscopy experiments of an exploratory nature will be shown in the section on Cu_xS.

4.2 Ion Damage

A convenient method for preparing thin electron transparent films of materials difficult to thin otherwise is the technique of ion milling. The surface of a pre-thinned specimen is bombarded with argon ions accelerated in a field of up to 10 kV. In most covalent substances, this produces only minor surface damage leaving the bulk of the material unaffected. It was found that all of the CdS films thinned by ion milling showed a very high density of small defects as shown in Fig. 4.3. In order to investigate the possibility of this defect structure being an artifact, a sample of bulk single crystal CdS as grown from the melt was thinned chemically and examined in the electron microscope (shown in Fig. 4.4a). No defects of any kind could be found, as demonstrated by the clean extinction contours parallel to the edge of the foil. When the same specimen was then subjected to the same ion milling treatment as the previous vapor-grown films, the structure in Fig. 4.4b was observed. This

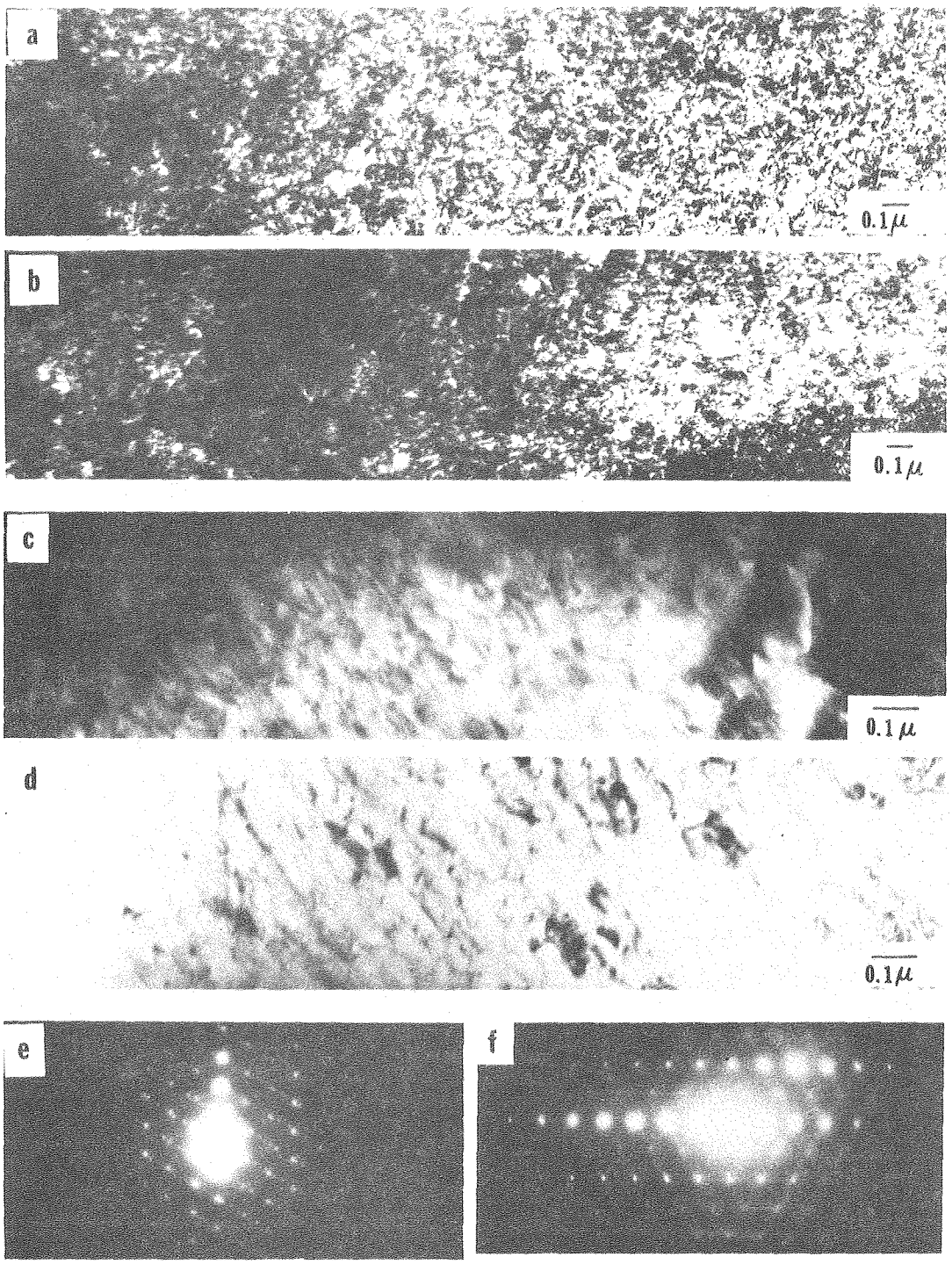

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Figure 4.3

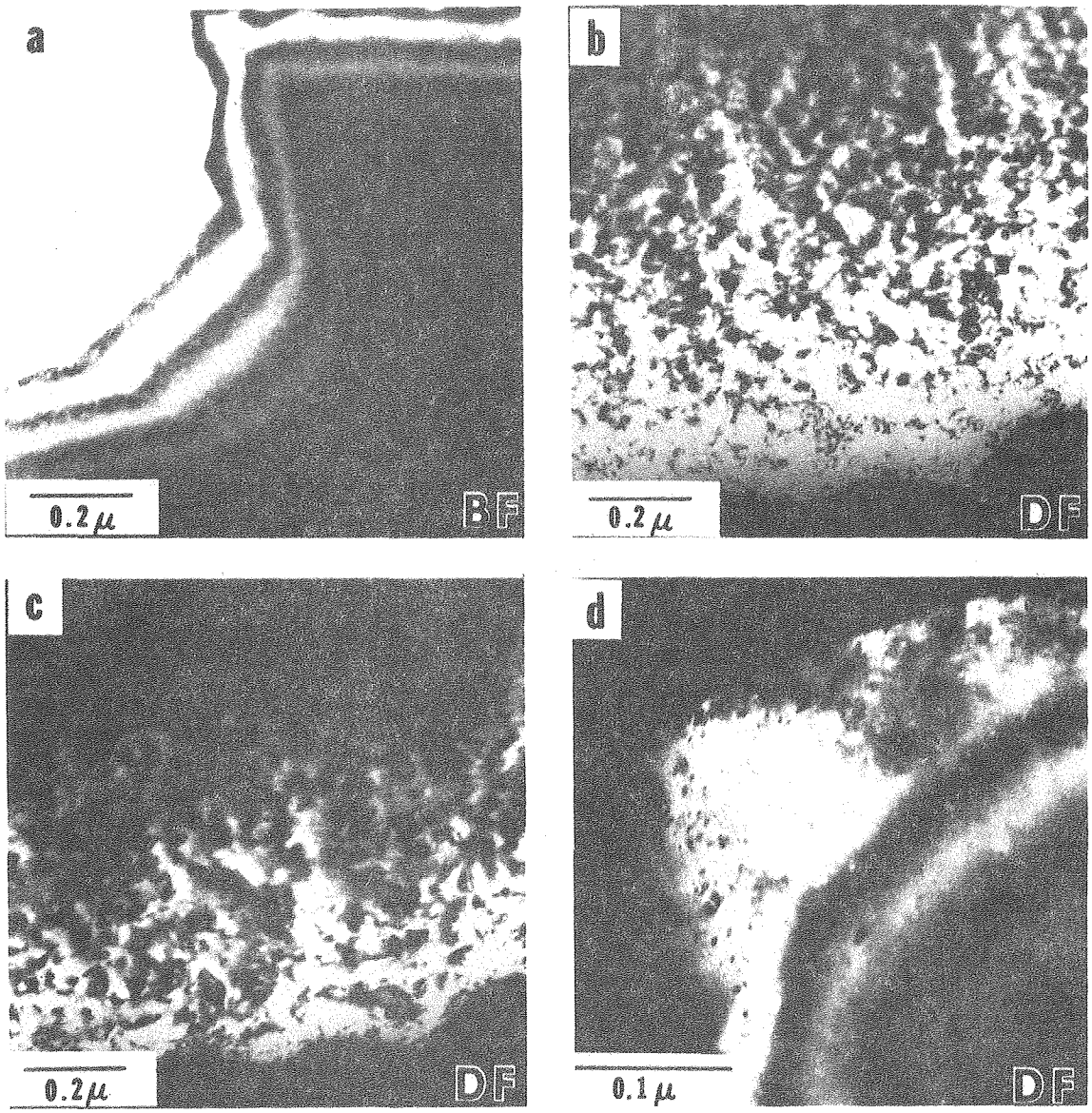

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Figure 4.4

structure is identical to the ones shown in Fig. 4.3 and is entirely due to ion damage. Subsequent ion bombardments at lower accelerating voltages reduced the density of defects but could not eliminate them completely even at 1.1 kV (see Fig. 4.4d).

In general, the process of ion milling depends on the energy transfer between an incident Ar-ion and a surface atom of the bombarded CdS. In an inelastic collision, enough energy is imparted to the Cd or S atom to remove them from the crystal surface. Usually, this "ion damage" is confined to a thin surface layer and does not affect the structure of the bulk crystal. Apparently there is a mechanism for CdS which allows the damage to extend beyond a thin surface layer. A possible explanation for this phenomenon is a combination of irradiation damage and a chemical reaction of the CdS with residual gases in the vacuum of the ion milling apparatus. Such a mechanism would be favored by the beam-induced heating of the specimen and is supported by the observation of second phases near the supporting Cu grid. Further evidence for a beam-induced chemical reaction is the fact that CdS films also deteriorate during observation in a 100 kV electron microscope, resulting in a background structure as the one shown in Fig. 4.2. However, the literature on radiation damage in semiconductors indicates that CdS has two distinct threshold energies for displacement by high energy electrons (115 keV and 300 keV),[19] both higher than the 100 keV of a standard electron microscope. Therefore, the observed background structure cannot be

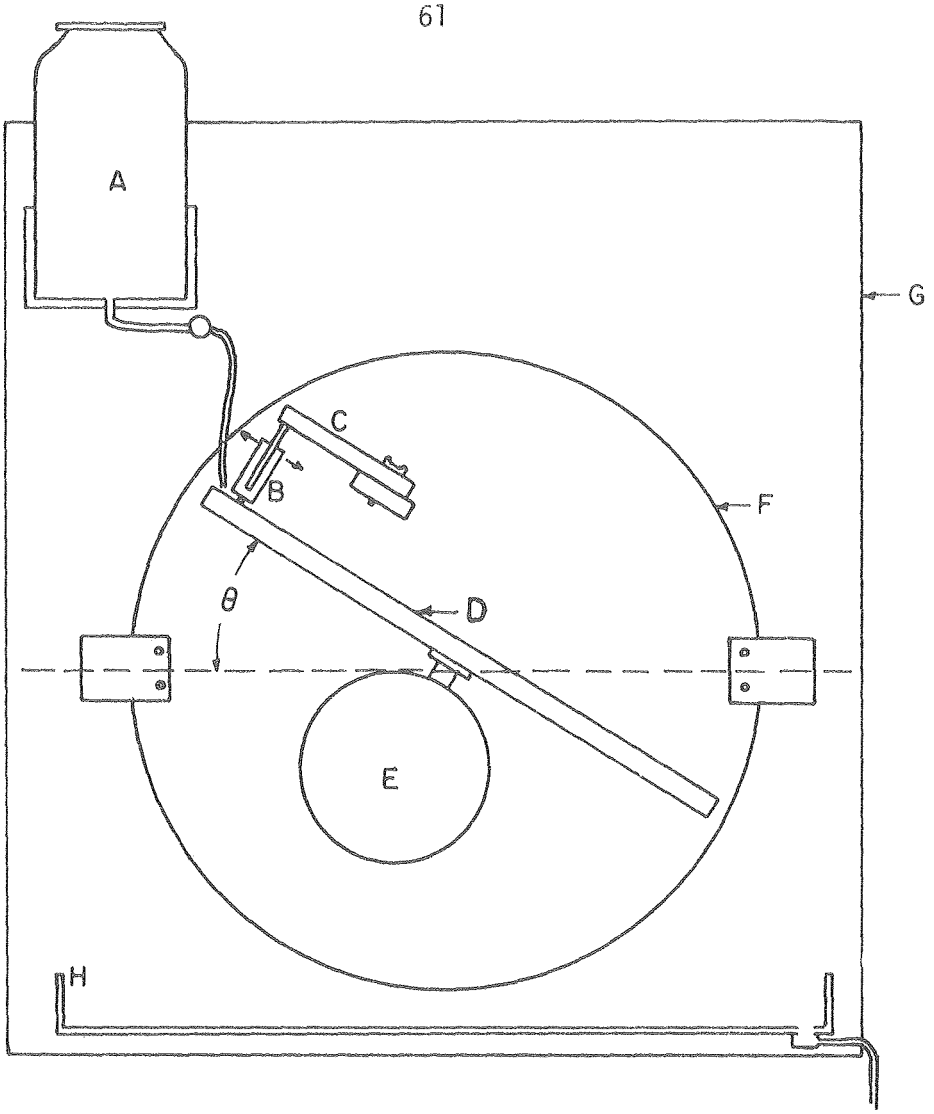
the result of simple displacement damage and must originate from a more complex process probably involving a chemical reaction.

In the absence of a more detailed understanding of the mechanisms responsible for the observed damage, it was decided that ion milling was unsuitable as a technique for thinning CdS for electron microscopy and a different technique using chemical polishing was investigated. The final technique is described in detail in the following section.

4.3 Preparation of Thin Foils for Transmission Electron Microscopy

Transmission electron microscope specimens were prepared by ultrasonically cutting 3 mm discs and mechanically thinning the Ge substrate to approximately 5 mils in thickness with 600 grit silicon carbide abrasive paper. The as grown CdS vapor deposited films were then thinned on the chemomechanical polishing apparatus shown in Fig. 4.5 (reproduced after Ref. 20). Specimens were mounted on the 7.7g teflon specimen holder. The polishing wheel which is 12 in. in diameter was covered with a polishing cloth (Buehler AB Selvyt) and was rotated at a speed of 85 R.P.M. Twenty percent HCl (volume percent of conc. HCl) was fed onto the polishing cloth at a rate of approximately 3 cc/min. Specimens were made at θ angles ranging from 15° to 68° with no difference in polishing results. Early specimens however polished on Leco Pan W cloth showed scratching at θ angles below 65°. The average thinning rate was 1.3 μ/hr.

After the CdS was thinned the specimens were masked with Lacomit Laquer leaving a 0.5 mm area of Ge exposed in the center of the specimen. The exposed Ge was removed by chemical polishing in a



A Acid Reservoir
B Specimen Holder
C Movable Support for Specimen Holder
D Polishing Wheel with Cloth
E Motor
F Rotating Mount for Motor, Wheel and Specimen Support
G Back Wall Support
H Drip Pan
θ Variable Wheel Angle

XBL7910-7238

Figure 4.5

gravity flow jet polisher. The polishing solution consisted of 87 pts. conc. HNO_3, 13 pts. conc. HF, and 50 pts. conc. acetic acid. The solution provided a reasonable polishing rate for the Ge (approximately 1,700 Å/sec.) and did not rapidly attack CdS.

The specimens were cleaned, then dipped for 1 sec. in 2 pts. conc. HNO_3, 1 pt. conc. HF, and 2 pts. conc. acetic acid to remove any possible surface damage caused by the chemomechanical polishing. Specimens were also prepared by dipping them in this solution prior to the Ge removal.

4.4 Polycrystalline CdS

In order to compare the microstructures of single crystal CdS grown at this laboratory with polycrystalline CdS films produced by other investigators studying CdS/Cu_xS photovoltaic cells, films prepared by the Westinghouse and University of Delaware research groups were examined with the following results.

When vapor deposited polycrystalline CdS films after etching in HCl are examined in the SEM (Figs. 4.6a and b) features 1-10 μ in size are observed. These are usually interpreted as high angle grain boundaries. Etching these films in H_3PO_4 at 180°C provides somewhat better delineation of the grain boundaries; however, features smaller than 1 μ are usually not reported. When examined by TEM however, these polycrystalline films, besides the various high angle boundaries (Fig. 4.6c), also showed small angle boundaries (Fig. 4.6d).

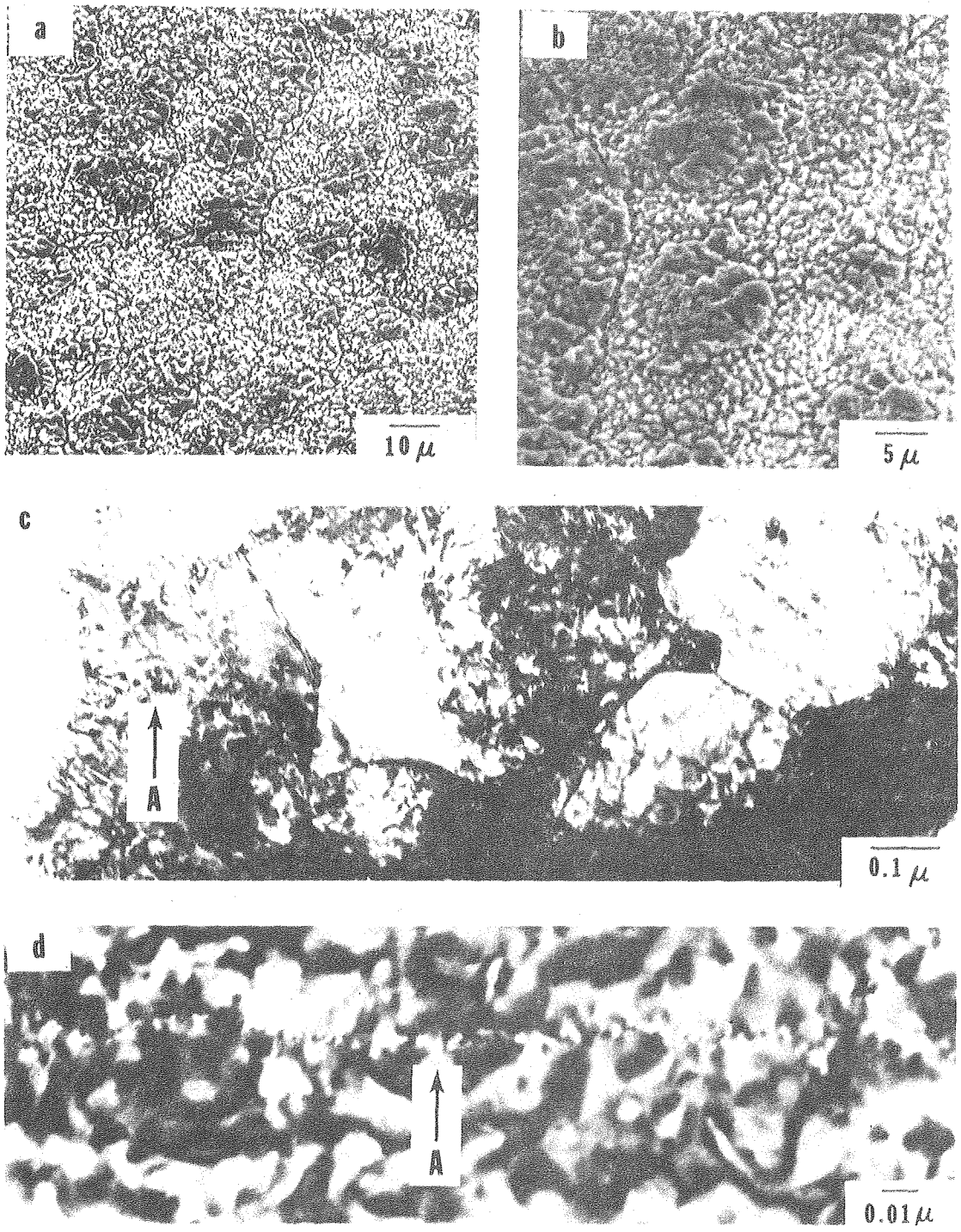


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Figure 4.6

Electron diffraction patterns obtained from a Westinghouse CdS film (sample #478) confirmed that the top layers of the film were being examined; this is because a highly oriented (002) ring pattern (Fig. 4.7b) was obtained in which those rings not belonging to this zone were absent. When a smaller aperture was used, a nearly single crystal pattern resulted (Fig. 4.7a). Notice however that some spots are rotated by a small angle (~10°). This diffraction pattern was obtained from the area shown in Fig. 4.8a and over the boundary marked A. A is therefore a boundary between two parts of the crystal which are rotated with respect to each other. The distance between dislocations required to accommodate a misorientation of 10° is about 17 Å; this corresponds to the distance between the dislocations in Fig. 4.8c. Figure 4.8b shows another boundary marked C which appears to be more or less perpendicular to the foil plane.

These high magnification images show that besides the high angle grain boundaries, there exist many small angle boundaries accommodating small misorientations. These subgrains are all less than 1 μ, and are typically of the order of 0.1 μ in dimension.

The films provided by the University of Delaware group were very similar in microstructure (Fig. 4.9). Fine grains of about 0.2 μm in size were separated by small angle grain boundaries as evidenced by the small change in contrast when crossing a boundary. In addition, long dislocations as observed in the single crystal films are seen to traverse the grains (see arrows in Fig. 4.9). Note that the strongly mottled background structure present in Figs. 4.6 and 4.8 is absent.

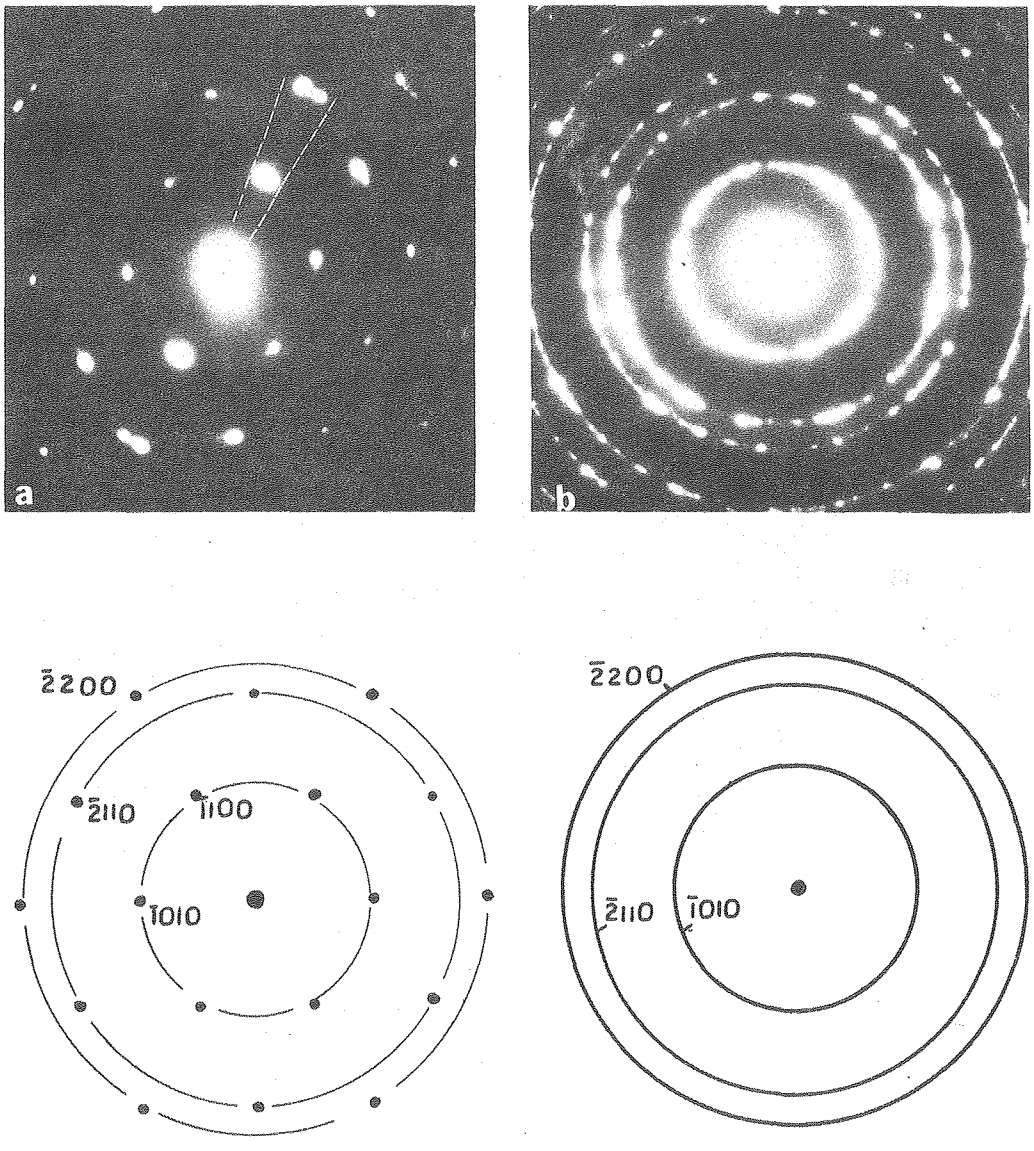

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Figure 4.7

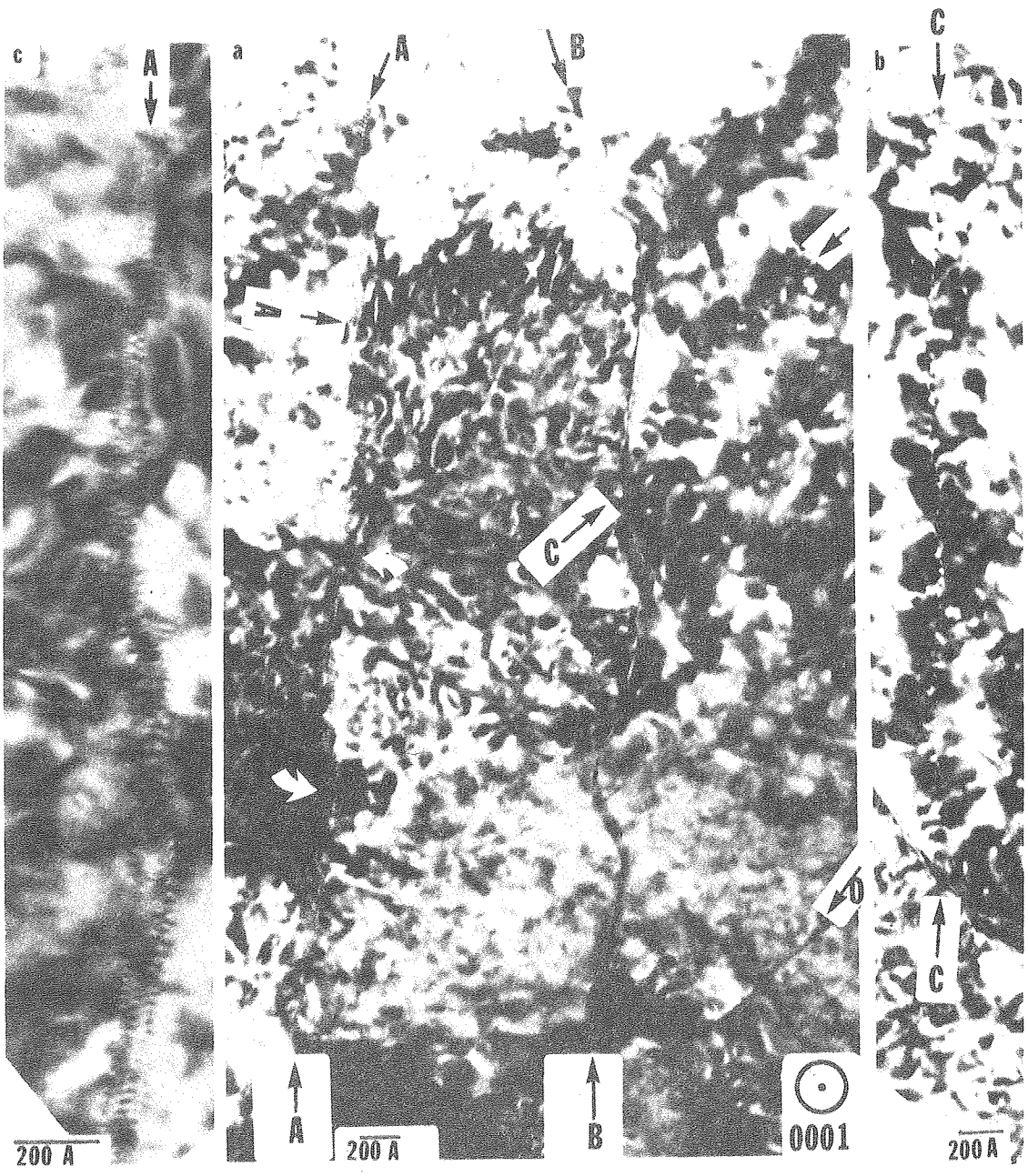

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Figure 4.8

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Figure 4.9

This is due to the fact that this film was prepared for electron microscopy by chemical rather than ion thinning. It is clear then that the two different polycrystalline films made by Westinghouse and the University of Delaware are very similar in their defect structures; a result which is not surprising since both were vapor deposited onto Zn-plated Cu substrates. Both have subgrain boundaries on a much smaller scale than the grains detected by SEM. The grain interior shows a dislocation structure which is compatible with the structure of the single crystal films described earlier.

4.5 Different Methods of Cu_xS Formation

In this section, a number of preliminary experiments are described which were designed to scan the various ways in which Cu_xS can be formed on CdS as required for heterojunction fabrication.

a. Reactive sputtering

Figure 4.10 shows the microstructure and diffraction pattern obtained from a single crystal CdS film which was reactively sputter-deposited with Cu_xS by the Lawrence Livermore Laboratory. The extra spots due to the Cu_xS layer are readily visible in the electron diffraction pattern (Fig. 4.10b) and indicate that the Cu_xS had been deposited epitaxially. When Cu_xS was reactively sputtered onto carbon coated electron microscope grids, the microstructures shown in the electron micrographs in Fig. 4.11 were obtained. Two different samples were examined; one with larger grain size (Fig. 4.11a,c) and one with smaller grain size (Fig. 4.11b,d). In the latter sample, these grains appear to have planar faults (Fig. 4.11d),

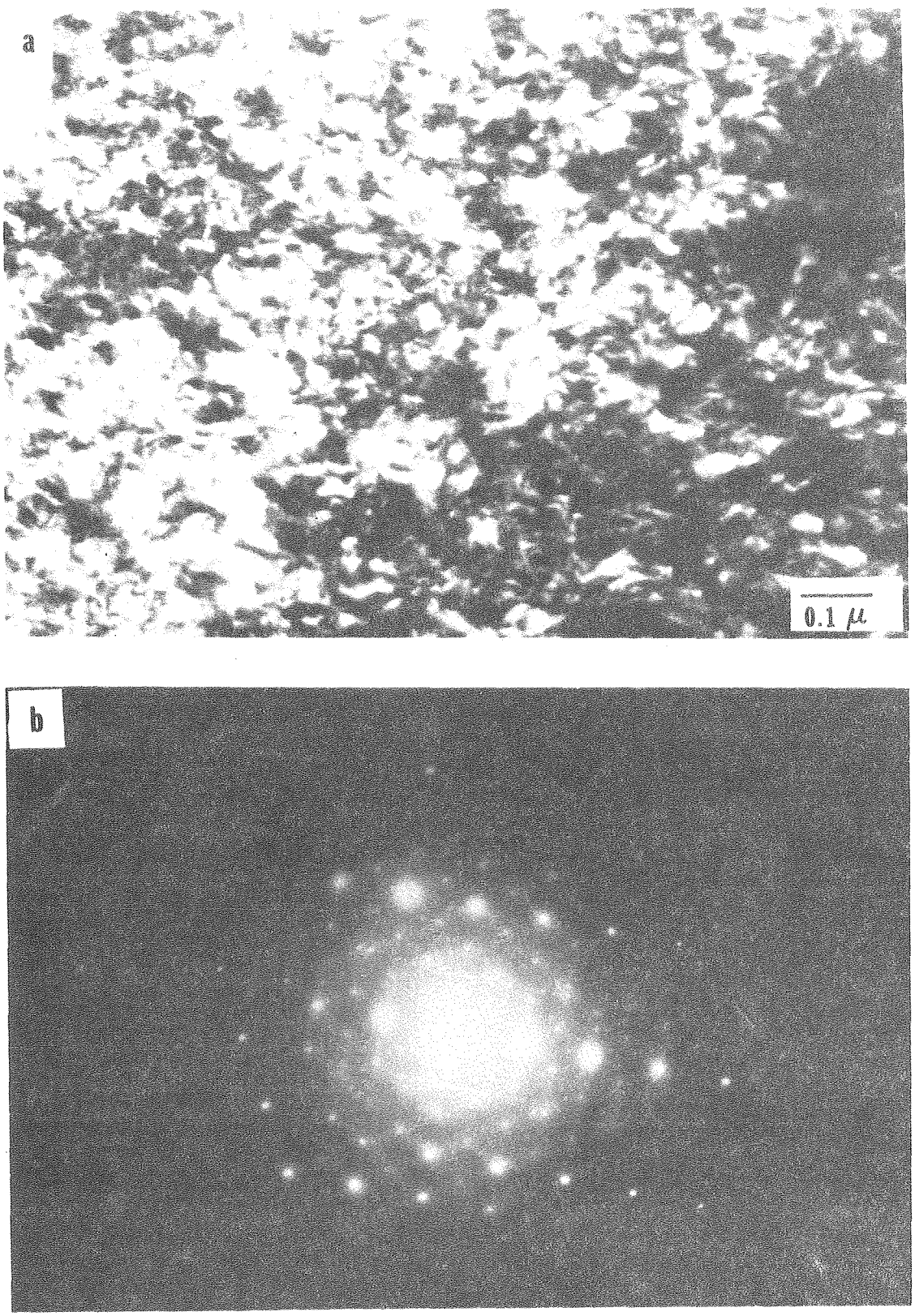

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Figure 4.10

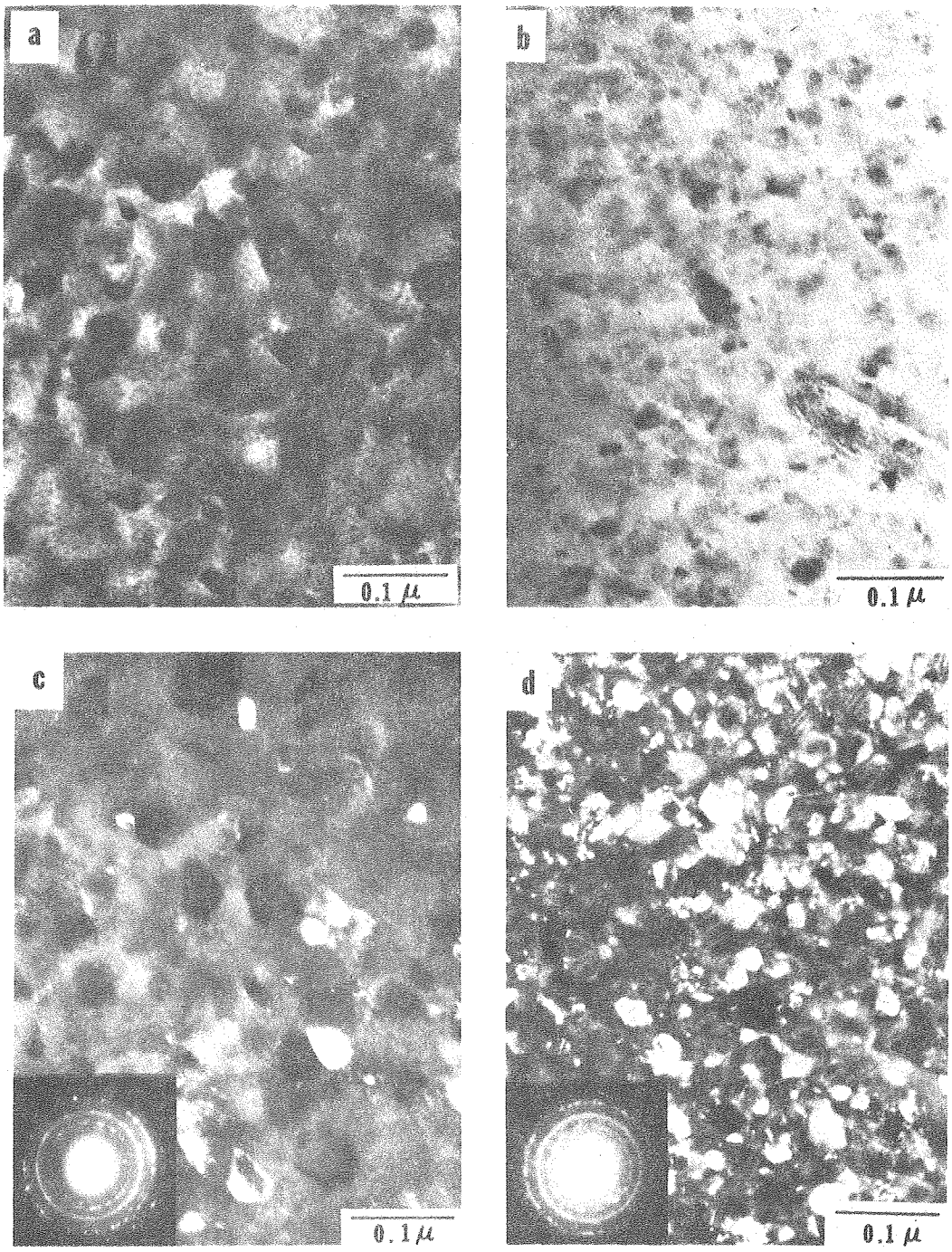

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Figure 4.11

which are absent in the other sample. In the same geometry, the two samples differed in electrical resistance by a factor of 50. This may be interpreted as either different Cu_xS phases being present in the two samples giving rise to the change in resistivity,[21] or the effect of grain size.

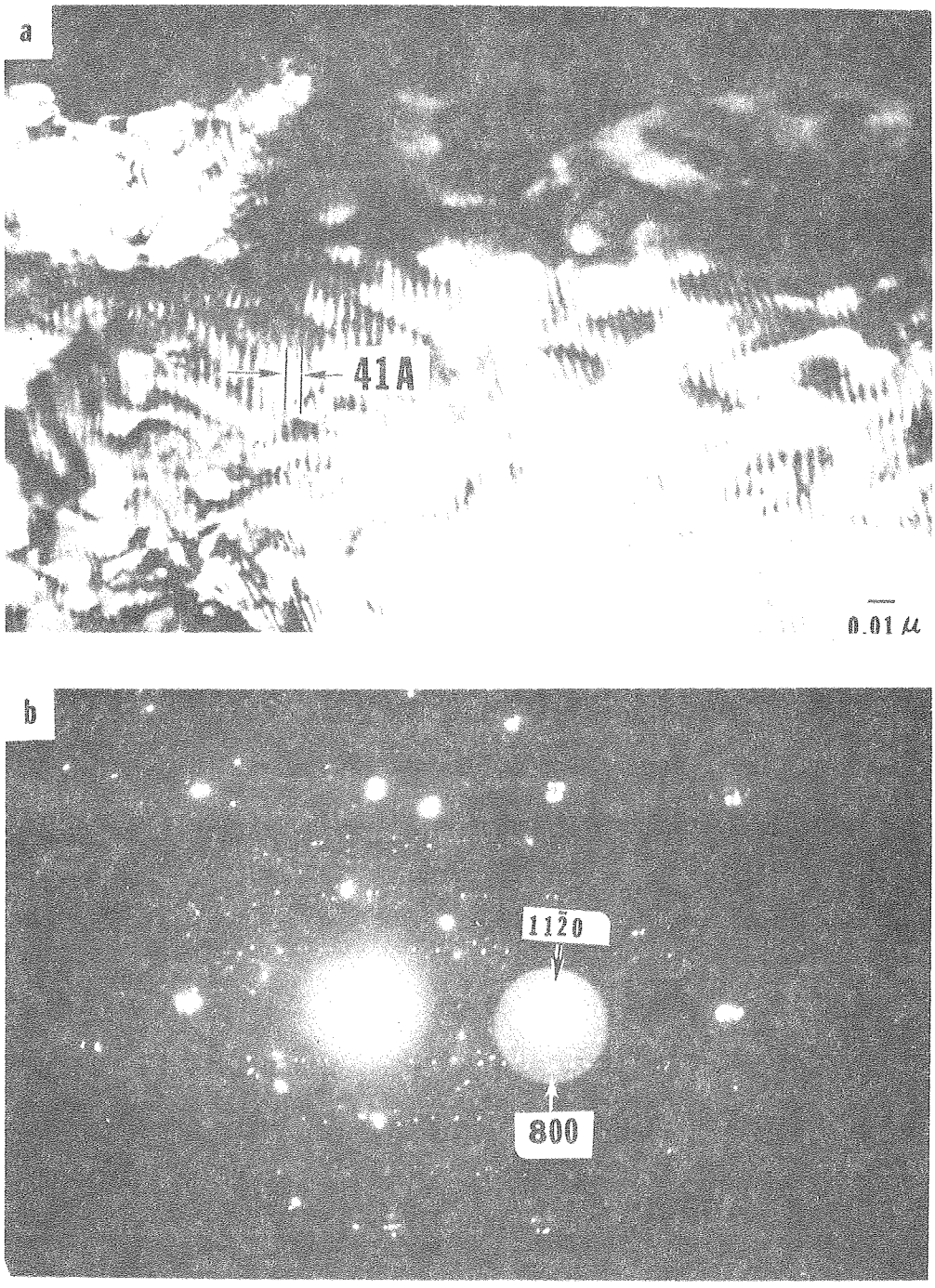
b. Ion-Exchange Method

A single crystal CdS film was dipped into a copper chloride solution held at 90°C and examined after slight ion milling. Figure 4.12 clearly shows the Moiré fringes arising from the topotaxial layer of Cu_xS with a spacing measured to be about 40 Å. This spacing corresponds to parallel Moirés produced by the difference in spacing of the $(11\bar{2}0)$ CdS and the (800) Cu_xS spots (see Fig. 4.12b).

This figure is an example of how previously characterized thin films of CdS or (Cd,Zn)S may be partially converted to Cu_xS. Because of the topotaxial relationship, a single crystal diffraction pattern as in Fig. 4.12b will be obtained which may be used to identify the local structure and morphology of the Cu_xS. Work anticipated for the future is to perfect this technique and proceed along similar lines for polycrystalline samples. A more detailed example of this type of local identification of phases is discussed below.

c. CdS Doped with Cu at the Growth Temperature

This sample was provided by the Westinghouse group and was prepared as follows: the proprietary coating on the copper substrate



XBB 787-8123

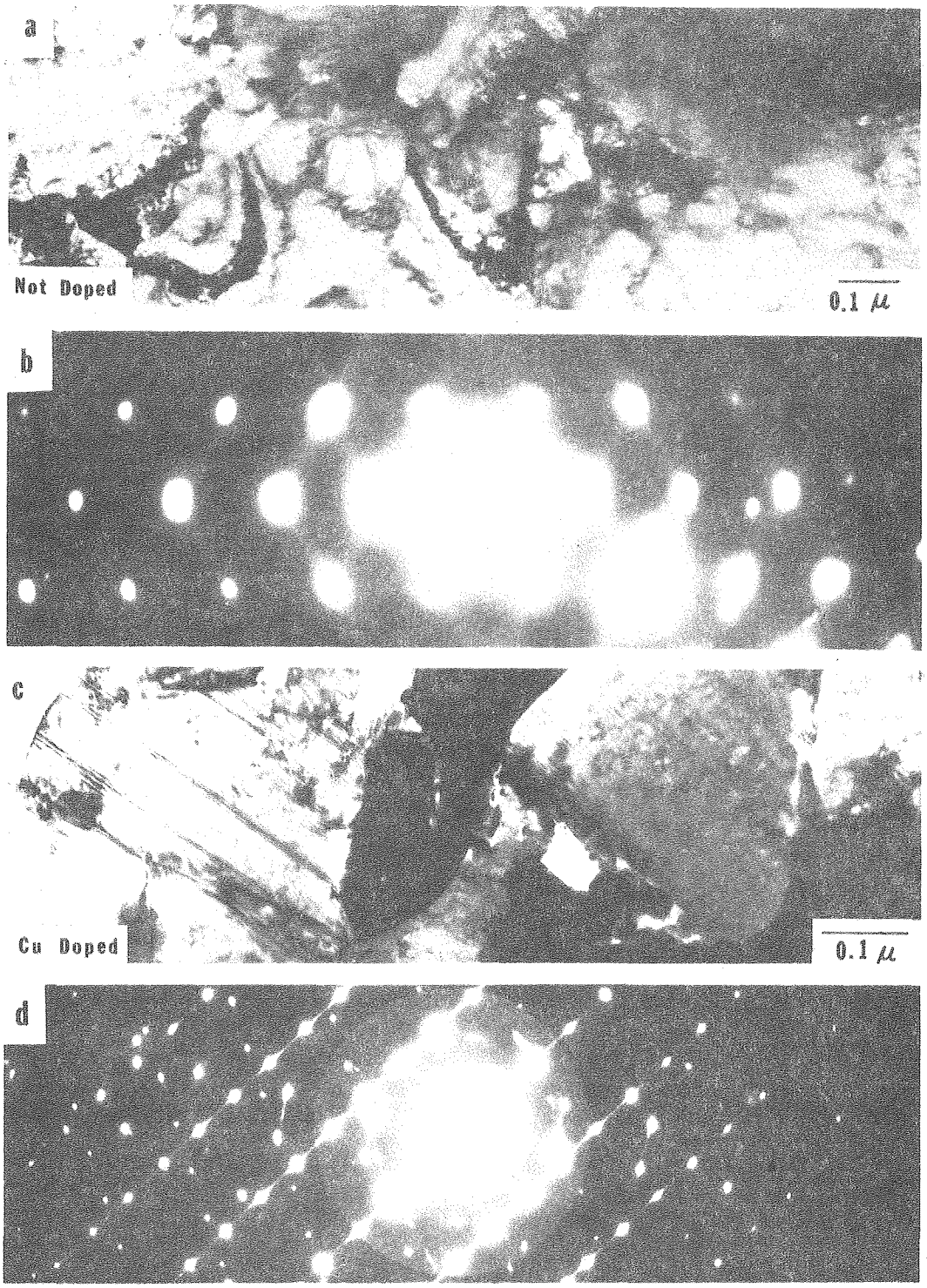
Figure 4.12

sheet was stripped by chemical etching, and CdS vapor deposited on this surface. Upon cooling the film was black, presumably from the diffusion of Cu into the CdS film during growth. Preliminary SEM-EDAX work showed that the sample had not been completely converted to cuprous sulfide.

When this film was ion-milled and examined by TEM, it was found to be profusely faulted. The electron diffraction pattern showed streaking in the $\langle \bar{1}010 \rangle$ directions indicating that the faults lie on the $\{\bar{1}010\}$ prism planes. Figure 4.13 compares the bright field image and the diffraction pattern of an undoped CdS film (Fig. 4.13a,b) with those from a doped film (Fig. 4.13c,d). Notice that when no copper was added, there were no faults or streaking in the electron diffraction pattern.

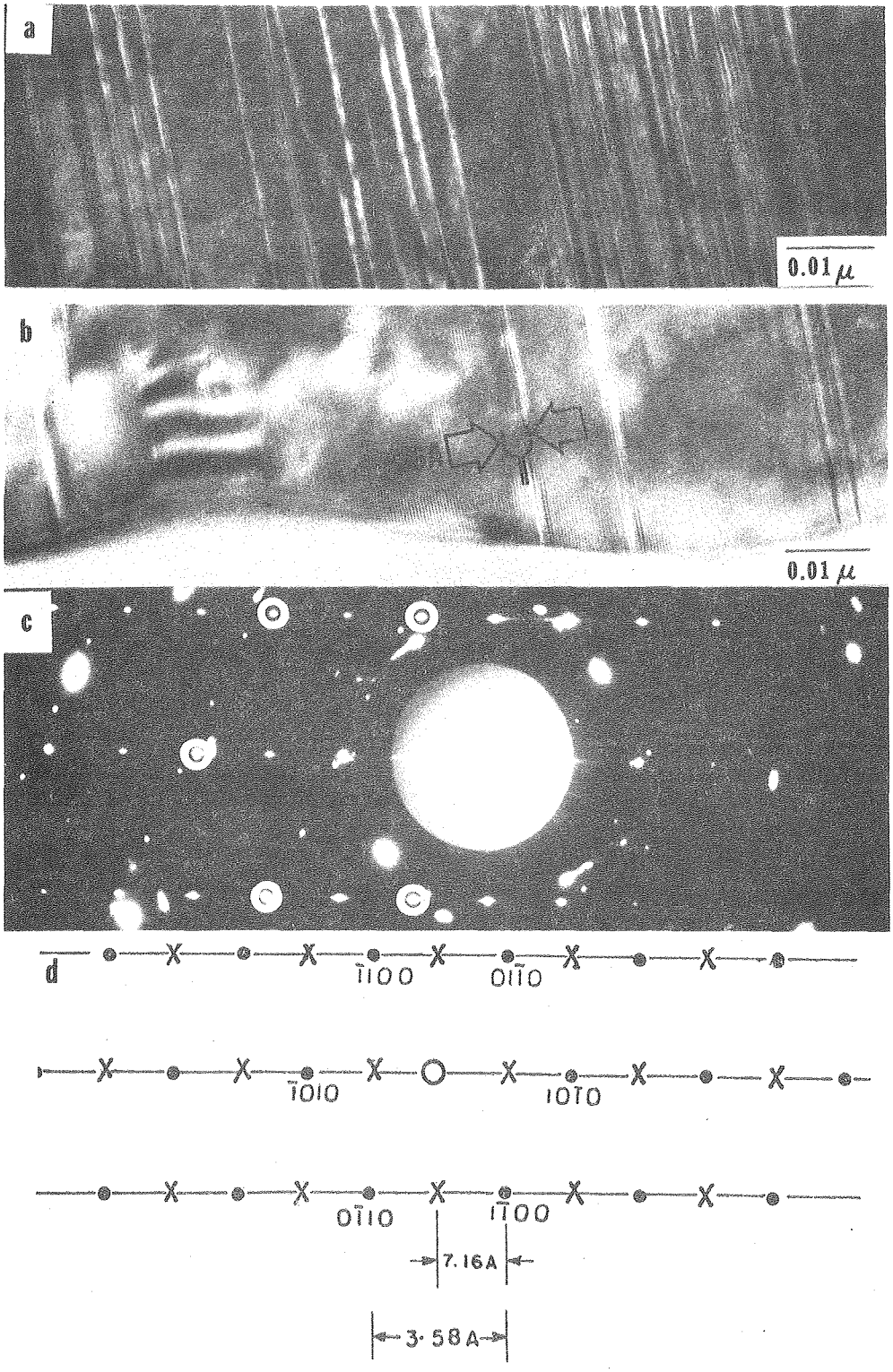
When the diffraction pattern was analyzed (Fig. 4.14c,d), it was found that besides the streaking through the $\{\bar{1}010\}$ type spots, extra spots appeared halfway between them (Fig. 4.14d). The distance between the spots corresponds to a spacing of 7.2 Å. Figures 4.14a and b show a bright field and lattice image of these planes with no marked interruptions of the fringe spacing found. It was concluded that the platelets were probably Cu precipitates arranged in a nearly periodic manner, rather than polytypes of CdS.

The nature of various kinds of faults in the sphalerite structure has been described by Holt[22] as shown in Fig. 4.15. The antiphase boundary (APB) of Type II is synonymous with a thin platelet of precipitate. It is likely that faults of this kind may be formed when



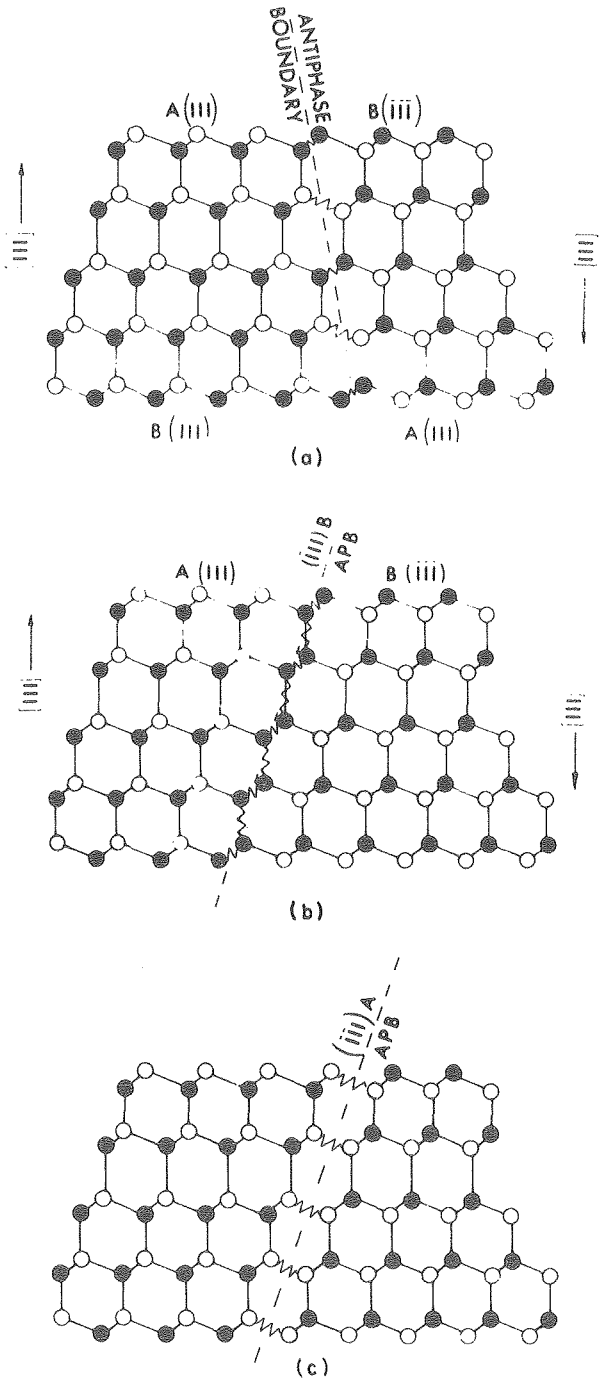
XBB 786-6983

Figure 4.13



XBB 786-7479

Figure 4.14



Antiphase boundaries in the sphalerite structure [$(1\bar{1}0)$ projection]. Zig-zag lines denote wrong bonds. (a) Type I APB on $(\bar{1}\bar{1}3)$ plane; (b) type II APB on $(\bar{1}\bar{1}1)$ involving wrong B–B bonds only and an excess of B atoms; (c) type II APB involving wrong A–A bonds with an excess of A atoms (Holt, 1969).

XBL 786-9204

Figure 4.15

copper is diffused into a polycrystalline CdS film. Note that APB's of Type II result in a change of the polarity of the crystal surface (Fig. 4.15b,c). Since such faults could occur on a fine scale in polycrystalline films, it is possible that the difficulty in determining the polarity of polycrystalline CdS by etching may be a direct result of faults of this kind. In addition to Type II APB's, it is also likely that APB's of Type I exist in CdS. These have lower energy than Type II faults and would appear in TEM as dark wavy lines. These results may provide further information as to the role of Cu diffusion in the ion-exchange conversion process in forming Cu_xS.

5. Electrical and Optical Measurements

5.1 Hall Effect Measurements

Hall Effect experiments were conducted on CdS films grown in the Van der Pauw geometry to obtain values of Hall mobility parallel to the substrate surface ("in-plane"), carrier concentration and resistivity. These electrical results were then correlated with structural information as obtained by TEM of these same films and also with their growth conditions. The results are summarized in Table 5.1 in which the Hall mobilities were measured at room temperature with a magnetic field of 6 KGauss.

An order of magnitude variation in Hall mobilities was observed with the lower values obtained from the polycrystalline samples. Because of the differences between substrate orientation and growth conditions, more specific relationships could not be determined. It should be noted, however, that despite the dislocations observed in these grown films (as discussed in Section 4), the carrier mobilities compared well with other measured values as listed in Table 5.1. The role of grain boundaries and surfaces,[23] and stacking faults[24] on the electrical properties of polycrystalline CdS has been discussed by Kazmerski, Berry and Allen. An empirical model was developed to explain the scattering effects of these defects. It was concluded that the fabrication parameters, especially the deposition rate and substrate temperature, determined the nature of the crystalline imperfections and therefore the electrical properties.

Table 5.1.

Hall Effect Measurements

Sample	Substrate	Growth Rate Å/μmole)	Crystallinity	Hall Mobility (cm^2/V-sec)	Carrier Concentration (cm^{-3})
2148	(111) Ga face	—	Single Crystal	44.6	10^{16}–10^{17}
6208	12° off (111) Ga face	65.89	Single Crystal	128.5	1.4×10^{17}
6158	($\bar{1}\bar{1}\bar{1}$) As face	21.40	Polycrystalline	13.8	2.7×10^{16}
6218	($\bar{1}\bar{1}\bar{1}$) As face	23.30	Polycrystalline	20.3	5.2×10^{16}
a	(111) Ga face	(~ 3,000 Å/min)	Single Crystal	125 - 154	5.4×10^{17}–1.7×10^{19}
b	Corning 7059	(40–400 Å/min)	Polycrystalline	11.1 - 16.0	10^{15} - 10^{16}

References

a – A. Yoshikawa and Y. Sakai, Japan. J. Appl. Phys. 13, 547 (1974).

b – L. L. Kazmerski, W. B. Berry and C. W. Allen, J. Appl. Phys. 43, 3515 (1972).

Yoshikawa and Sakai[15] reported that CdS films grown on GaAs substrates in H_2 gas by the close-spaced technique resulted in films with low resistivity and carrier concentrations as high as 5×10^{19} cm^{-3}. They found for films grown at substrate temperatures of 750°C for 10 min. that the dominant donor species was Ga which had diffused from the GaAs substrate. Our Hall measurements made on single crystal and polycrystalline films grown on GaAs substrates showed carrier concentrations in the 10^{16}-10^{17} cm^{-3} range. This data along with the fact that the films were grown at substrate temperatures 300°C lower than that used by Yoshikawa and Sakai led us to believe that autodoping was not occurring.

Hall mobility measurements of two samples at room temperature were made at different magnetic fields to determine the effects of magnetoresistance. Figures 5.1 and 5.2 show the change in Hall mobility with magnetic field for samples 6208 (single crystal CdS) and 6218 (polycrystalline CdS), respectively. Note that the curves take the same form for both single crystal and polycrystalline samples. Beer and Willardson,[25] by taking into account mixed scattering from acoustic phonons and ionized impurities, have reported this same type of behavior for single crystal Ge. Since our measurements were taken at room temperature, scattering from both of these processes were probably present.

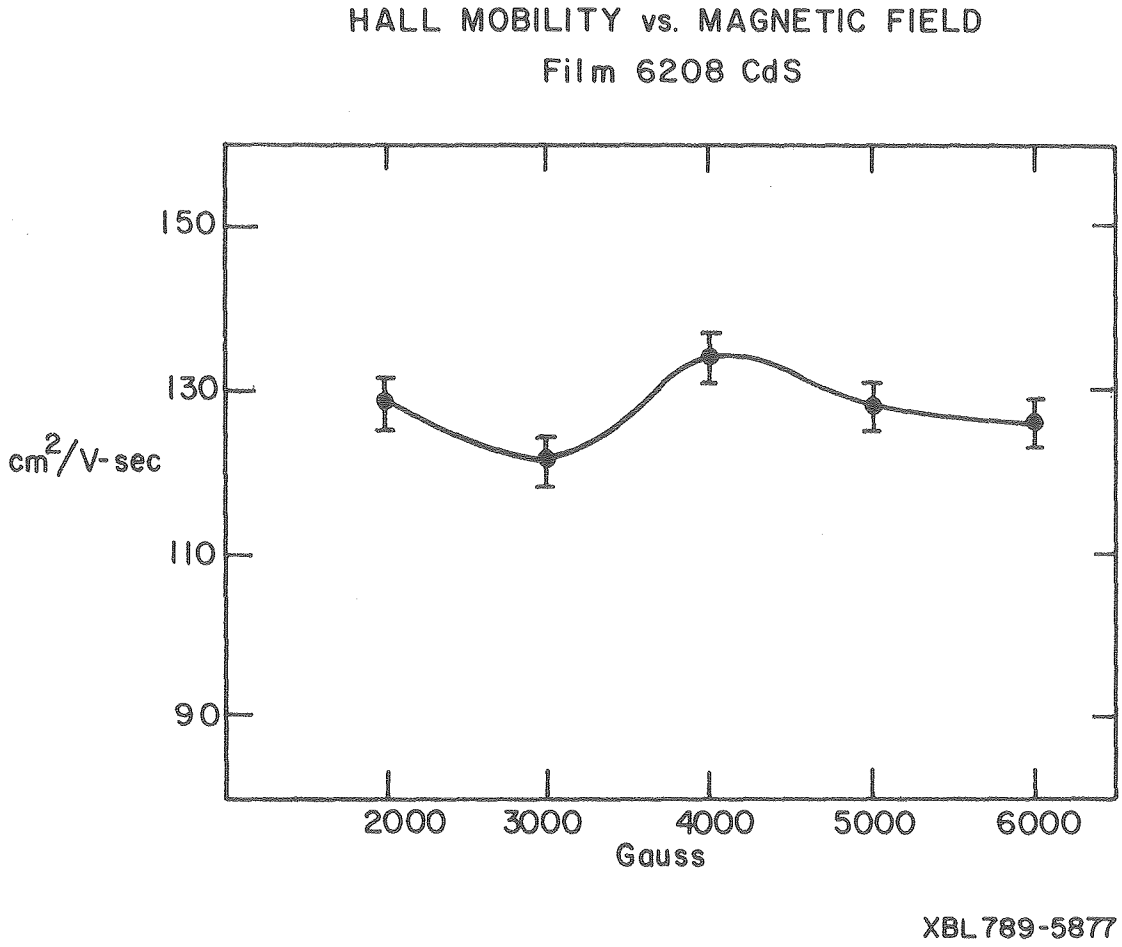

HALL MOBILITY vs. MAGNETIC FIELD
Film 6208 CdS
150
130
110
90
cm²/V-sec
2000
3000
4000
5000
6000
Gauss
XBL 789-5877

Figure 5.1

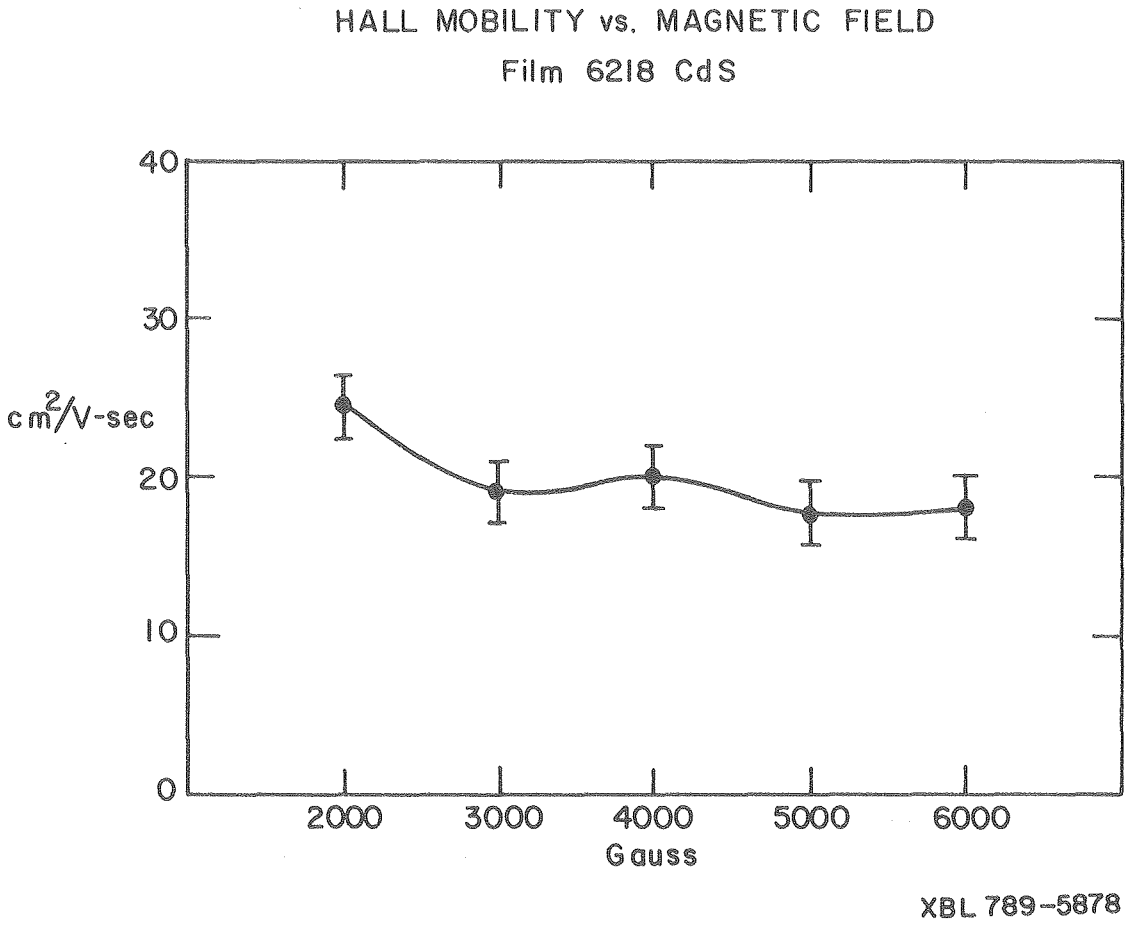

HALL MOBILITY vs. MAGNETIC FIELD
Film 6218 CdS
40
30
20
10
0
cm²/V-sec
2000
3000
4000
5000
6000
Gauss
XBL 789-5878

Figure 5.2

5.2 Heterojunction Fabrication

Figure 5.3 shows a schematic cross-section of a completed device, less contacts. The steps in producing this structure from the (Cd,Zn)S film grown on GaAs were as follows: (1) The surface of the film was polished to provide a planar interface, provided the film was thick enough ($\gtrsim 10$ μm) to withstand this treatment. (2) The surface was given a short etch in dilute HCl. (This step was not performed for early cells.) (3) CuCl was vacuum evaporated onto the surface through a mask. (4) The cell was heated in an argon or argon +2 percent H_2 atmosphere for times from 30 min. to 2 hrs. at between 130°C and 175°C. (5) The reaction products were washed off the surface in water and in methanol. (6) At this point silver paint contacts were formed on the Cu_xS layer and the GaAs to check that the device worked. (7) If the device gave a photovoltaic response in the "front-wall" mode in step 6, the GaAs was masked at the edges with enamel and etched away from the back of the (Cd,Zn)S film in chlorine bleach. (8) Finally, the silver paint contacts were remade. Table 5.2 shows the details of each step for the cells made on films grown on GaAs substrates. (The first segment of the cell designation denotes the CdS or (Cd,Zn)S film used as listed in Section 3.)

A few remarks about the ohmic contacts are in order here. The silver paint was adequate for contacting the Cu_xS layer; although when the Cu_xS was too thin there was a measurable photovoltaic (P.V.) response from the paint which formed a Schottky barrier with the mixed crystal. The contact to the (Cd,Zn)S presented more of a

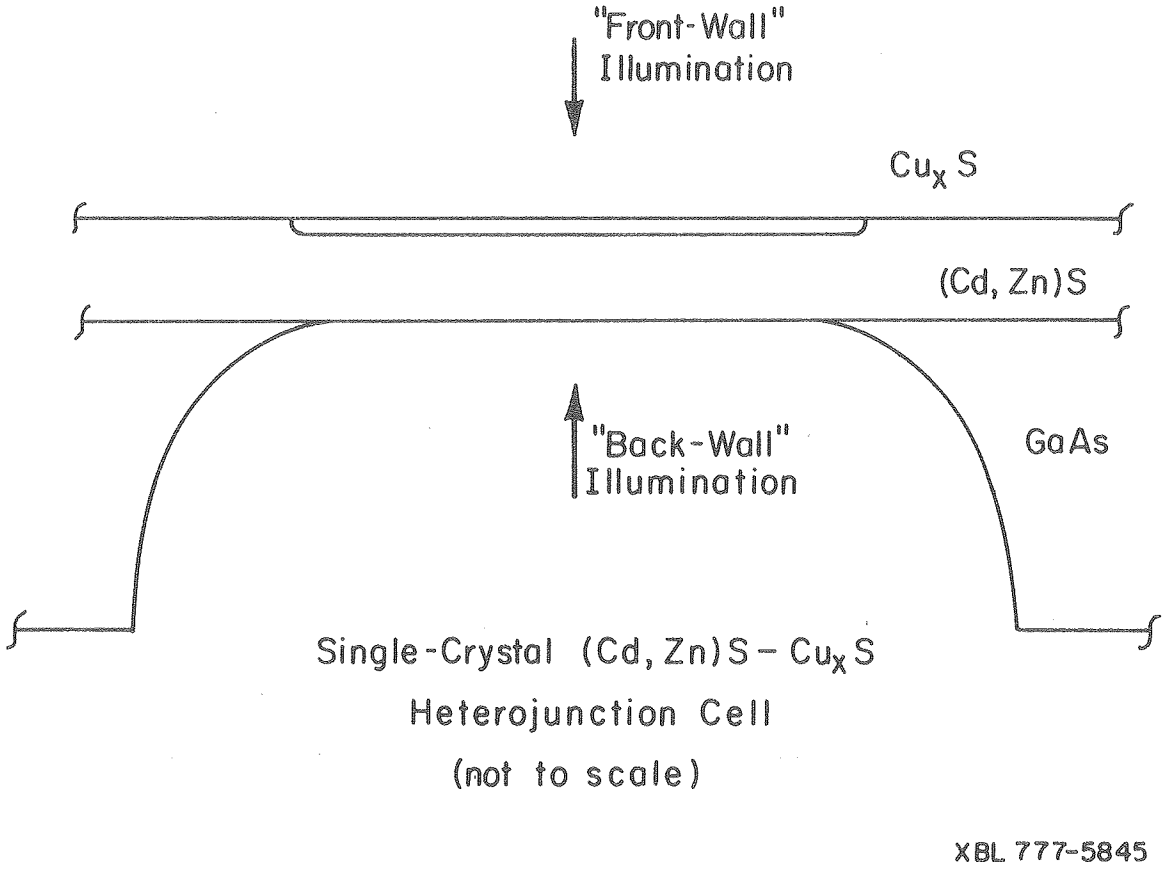

"Front-Wall"
Illumination
$Cu_x S$
(Cd, Zn)S
"Back-Wall"
Illumination
GaAs
Single-Crystal (Cd, Zn)S – $Cu_x S$
Heterojunction Cell
(not to scale)
XBL 777-5845

Figure 5.3

Table 5.2. Summary of Device Experiments for Films Grown on GaAs Substrates

Cell No.	Polish	Etch time/HCl conc.	Heat Tr. time-temp. (hrs.-°C)	I_{sc}^* W-lamp or (sunlight)	Voc* W-lamp or (sunlight)	ZnS fraction	Cu_xS Formation D = Dry Process S = Sputtered	Comments
10046-1	none	none	1.0 - 137 ± 3	.5 mA F .16 mA B	.41 V F .34 V B	0	D	CdS film
2047-2	1 μm C	5 min/25%	2.0 - 135	—	—	.29	D	Shorted
5247-1	none	none	0.5 - 170	~ 10 μA F	~ .1 V F	.15	D	Unstable-shorted after appl. of ~ 10 V bias
6167-1	none	5 sec/10%	0.5 - 180	24 μA F ~ 1.2 mA/cm^2 (15 μA F)	.48 V F (.38 V F)	.19	D	In contact to (Cd,Zn)S
6167-2	none	5 sec/10%	2.0 - 185	—	—	.19	D	Shorted
6177-1	none	5 sec/10%	2.0 - 185	—	—	.11	D	Shorted
6217-1	none	5 sec/10%	2.0 - 185	~ 1 μA	—	.17	D	High (~ .6V) barrier
1208-1	none	5 sec/10%	2.0 - 185	200 μA F ~ 10 mA/cm^2	.50 V F	0	D	Non-ohmic back contact - High R_S
9077-1	none	none	(3 min in Air @ 200°C)	21 μA F	.34 V F	0	S	Polycrystalline CdS
9077-1	none	none	(Add 3 min in Air @ 200°C)	40 μA F	.34 V F	0	S	Additional Heat Treatment
3088-1	none	none	(3 min in Ar @ 200°C)	2 mA/cm^2 F	.42 V F	.03	S	"Reverse-knee"

*F = Front-wall
B = Back-wall

problem, however. The GaAs could be contacted satisfactorily with silver paint, but since the GaAs-(Cd,Zn)S interface (at least with Zn-doped, p-type GaAs) behaved as a "leaky" diode, the overall contact resistance was too high. Indium was used to contact the front of the mixed crystal, but such contacts were not more effective because the film resistivity was too high to collect "in-plane" currents efficiently (see the results for cell No. 6167-1 in Table 5.2).

In order to use the substrate as an ohmic back contact for front-wall cells, n-type GaAs was used. It was not known if the n-CdS/n-GaAs heterojunction would be ohmic because of the uncertainty in the values of electron affinity (from Table 3.1 ΔE_c = .43-.80 eV) and also because of the effect of interface states. Experiments with n-GaAs substrates determined that this heterojunction also acted as a "leaky" diode. Ohmic junctions were obtained for CdS grown on n-type Ge substrates allowing for front-wall cell construction.

Cu_xS was deposited by reactive sputtering onto our CdS and (Cd,Zn)S thin films by the Lawrence Livermore Laboratory for comparison with the dry process. These heterojunctions were structurally (see Section 4.5a) and electrically characterized. The sputtering parameters in forming these Cu_xS films are described elsewhere.[26]

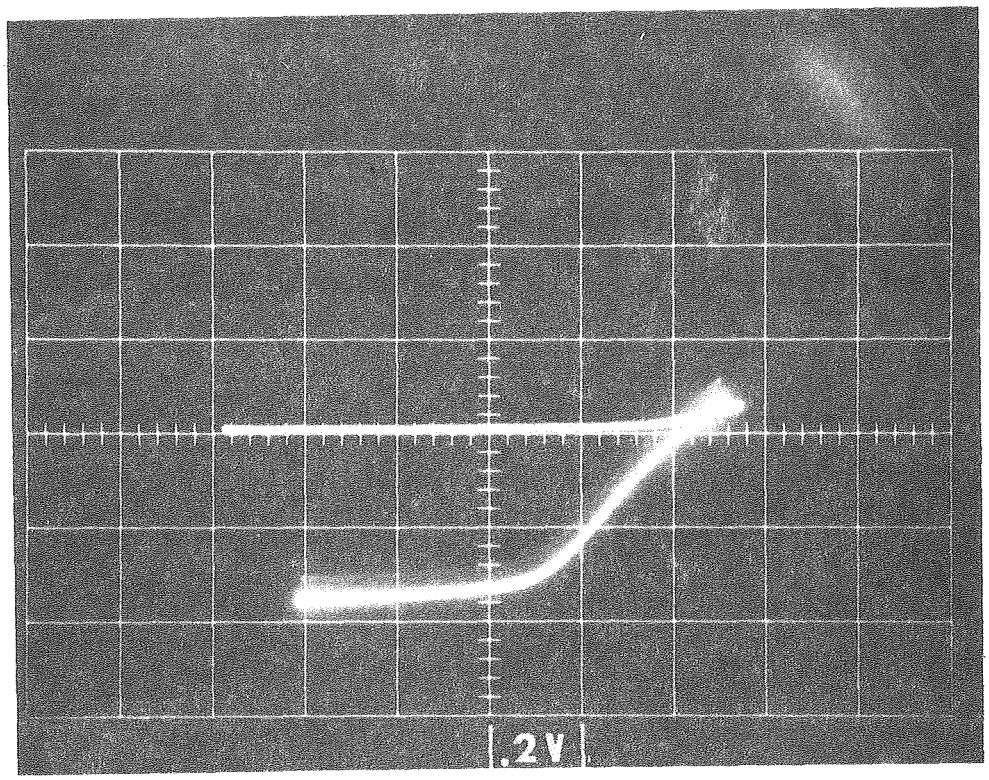
5.3 Current-Voltage Measurements

The I-V characteristics of a representative sample of cells using GaAs substrates are summarized in Table 5.2. As noted in the previous section, difficulties were encountered in using both p- and n-type

GaAs substrates because of the non-ohmic back junction for front-wall cells. This affected the illuminated I-V characteristics resulting in a "reverse-knee" as shown in Fig. 5.4. Front-wall tungsten lamp and sunlight I-V curves for a cell (6167-1) using an In contact to the (Cd,Zn)S are shown in Figs. 5.5a and b, respectively. (No attempt was made to simulate any sunlight-equivalent condition with the tungsten lamp. It was intended only as a reproducible experimental condition for comparison between cells). As discussed in the following section on spectral response measurements, the low currents measured were partly due to the insufficient thickness of the Cu_xS layers.

Many of the cells produced by the dry process using heat treatment temperatures greater than 100°C resulted in shorted devices. Figure 5.6 is an SEM micrograph of the top surface of a (Cd,Zn)S film (Run 9258) converted to Cu_xS by heat treating at 135°C for 1 hour. The cracks which were observed only after the conversion process are due to the difference in lattice parameter as reported by Singer and Faeth,[27] and Cook, Shiozawa and Augustine.[28] It is believed that these cracks provide a fast diffusion path for Cu resulting in short-circuits through the cell. Non-shorted cells using the dry process were possible for the thicker CdS or (Cd,Zn)S films.

To circumvent the shorting problems associated with the dry process, devices were also formed by reactive sputtering of Cu_xS. Some of these results are summarized in Table 5.2. Other experiments were performed in which the heat treatment temperature and time used for the dry conversion process was varied. Figure 5.7 shows the



Cu_xS- $(Cd_{.97}Zn_{.03})S$ Single Crystal Cell

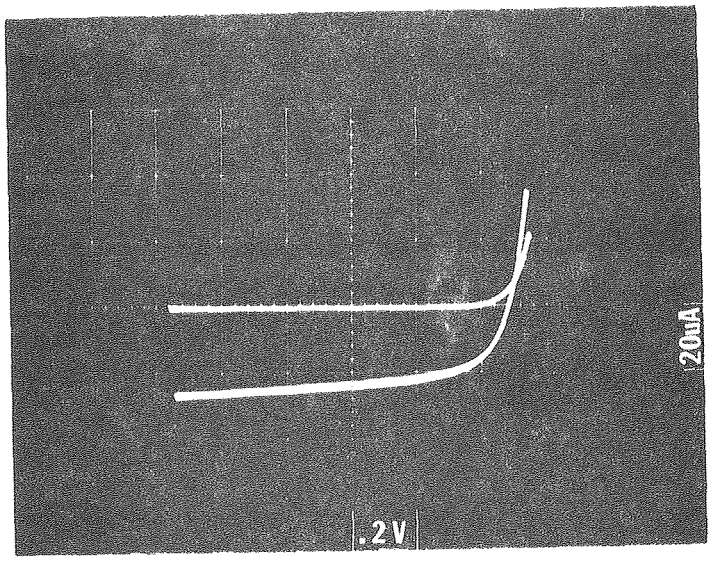
Cu_xS Sputtered by LLL

Under Tungsten Lamp Illumination

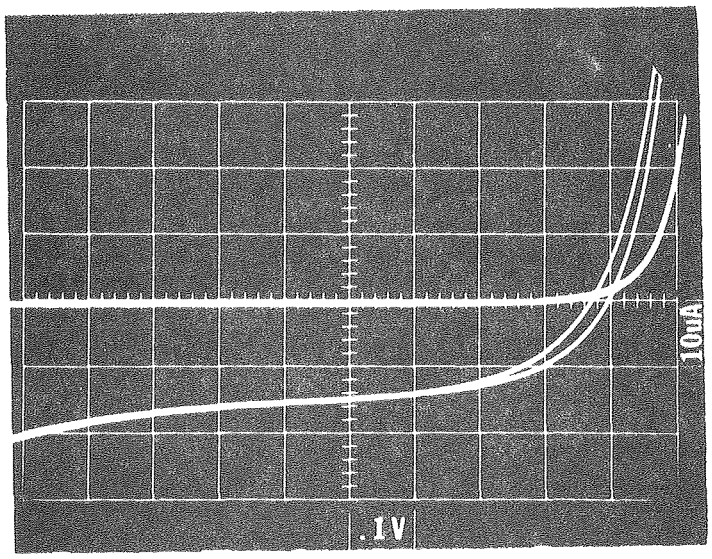
V_{oc}=.42V, J_{sc}=2mA/cm^2

XBB 784-4300

Figure 5.4



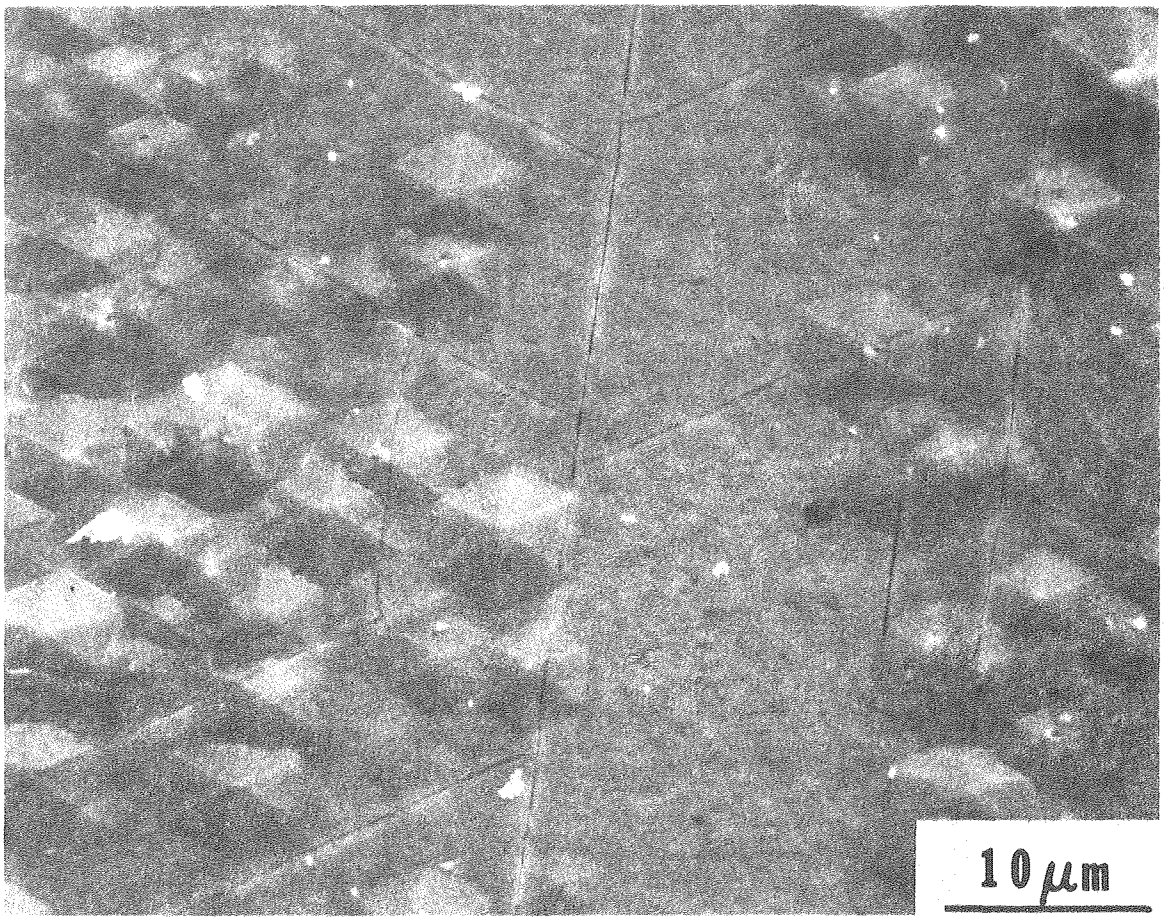
a



b

XBB 777-6683

Figure 5.5



XBB 7810-13124

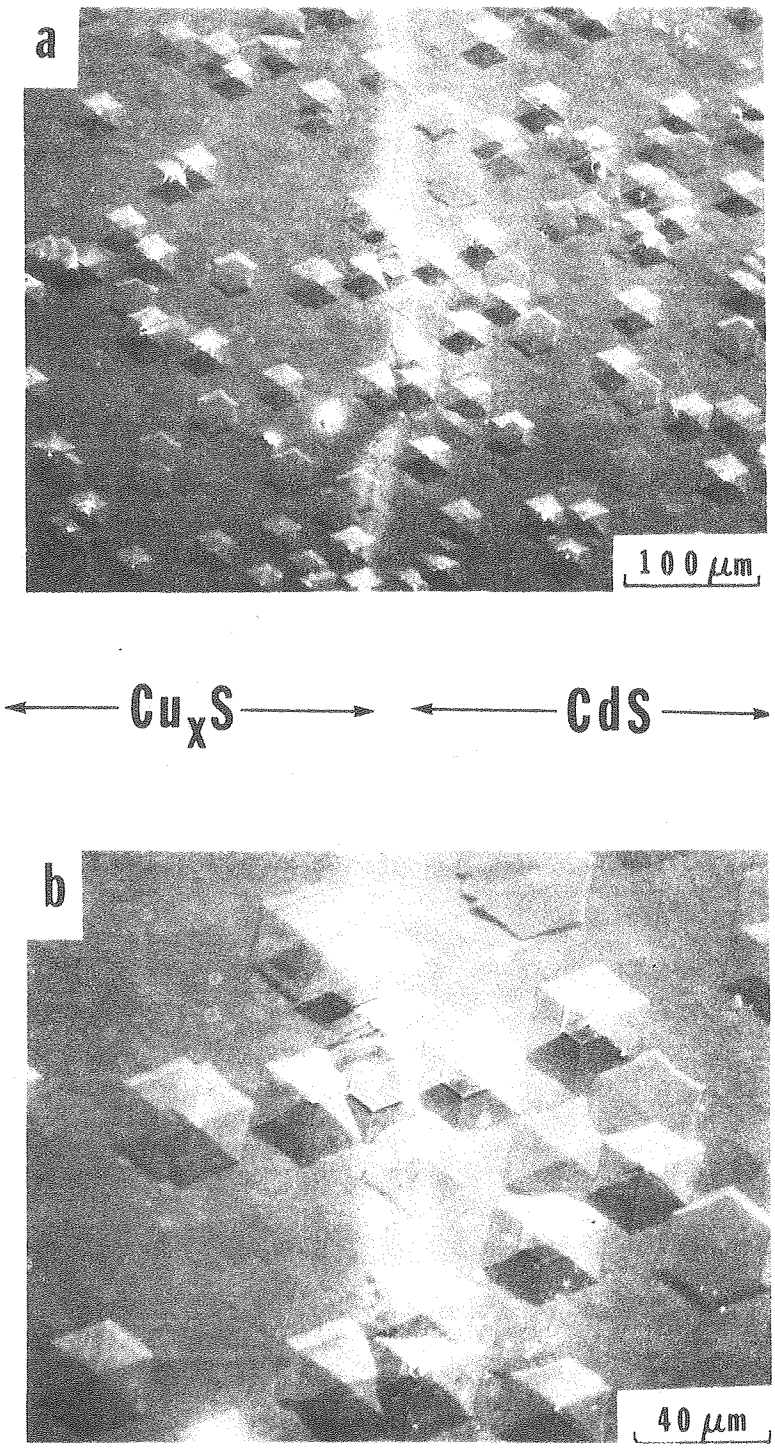
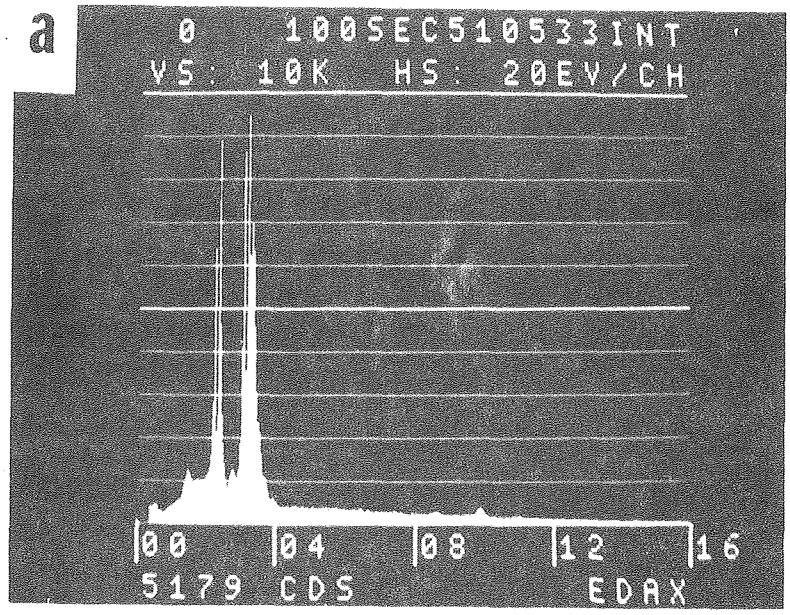


Figure 5.7

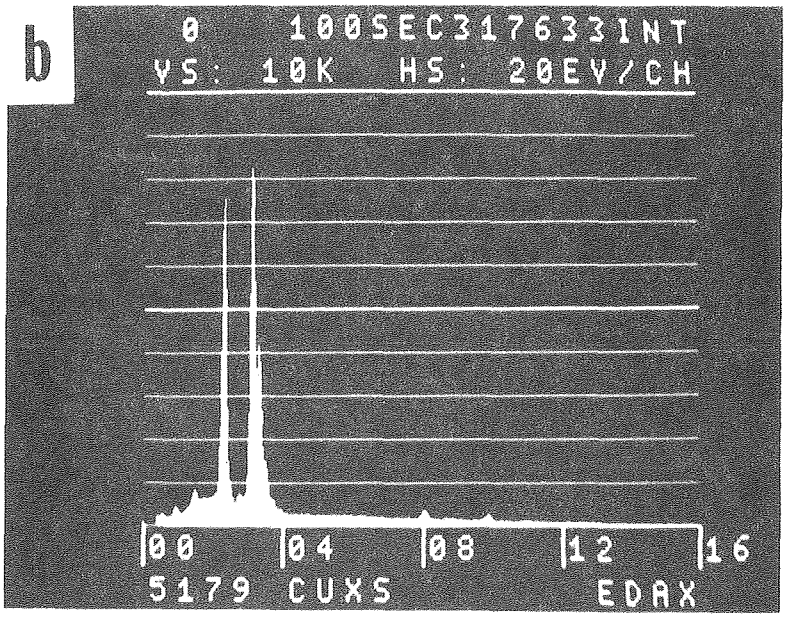
original CdS and converted regions using a heat treatment temperature of 60°C for 1/2 hour. No cracks were observed in this case for the entire surface. The converted Cu_xS region was checked using EDAX. Figure 5.8a is the EDAX spectrum of the area marked as CdS in Fig. 5.7, showing the characteristic lines for the elements S, Cd and Ge (from the underlying substrate). Figure 5.8b shows the presence of Cu which was detected only in the evaporated CuCl region which was converted to Cu_xS. The I-V characteristics of this cell are shown in Fig. 5.9b. When the conversion process was performed at 60°C for 1 hour on a different CdS film (8249), the short-circuit current increased while the open-circuit voltage decreased as shown in Fig. 5.9a. This may be explained by a thicker Cu_xS layer and hence larger generation of carriers but a higher shunt conductance was measured, resulting in a lower V_{oc}.

5.4 Spectral Response Measurements

A rather sophisticated apparatus for obtaining electrical and photo-electrical measurements on CdS/Cu_xS or (Cd,Zn)S/Cu_xS hetero-junctions is desirable because of the well-known difficulties involved in making reliable measurements of the properties of these devices. The design objectives of the apparatus used in this project were: (1) to allow for spectral response measurements using either monochromatic light with very low stray light levels or a chopped monochromatic beam together with "bias" illumination and (2) to obtain truly steady-state current-voltage measurements at temperatures between 77°K and 350°K and at any illumination (including zero). The



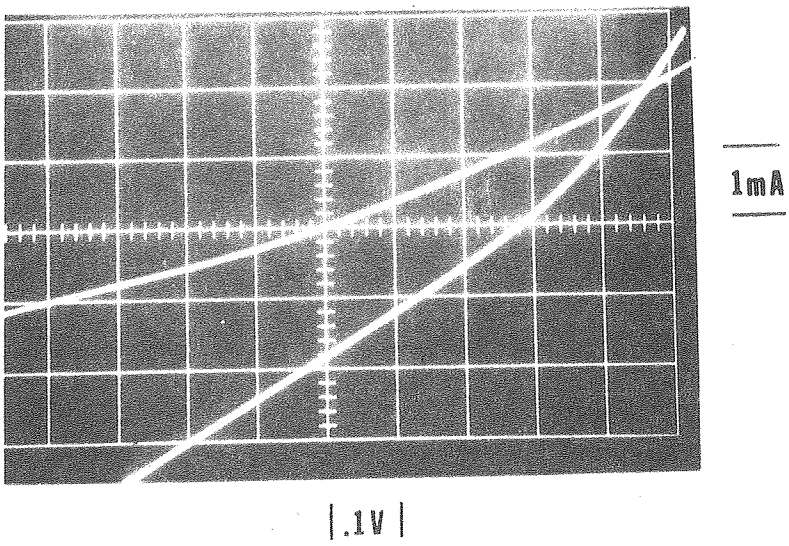
S Cd Ge



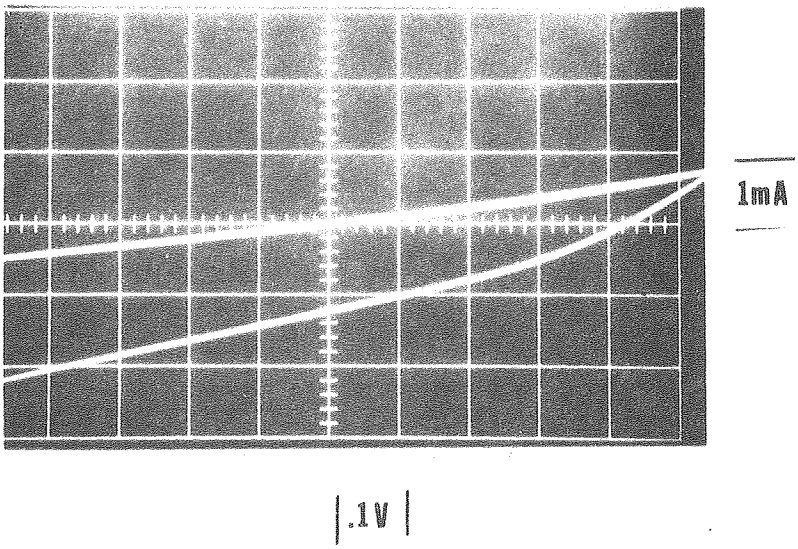
S Cd Cu Ge

XBB 790-15814

a. 8249A



b. 5179A



XBB 790-15813

Figure 5.9

motivation for the first objective is a need to study systematically the nonlinear "two-beam" effects found in these devices. The importance of the second objective is a result of the long-lived trapping states which give rise to very long relaxation times - especially in the dark - in the I-V characteristics of these heterojunctions.

Figure 5.10 shows a block diagram of the apparatus in the spectral response configuration. The system controller is an 8080-based microcomputer with a resident BASIC interpreter which allows great flexibility in control of the different experimental variables. The light source consists of a tungsten halide lamp, usuable to wavelengths down to ~ 350 nm, whose intensity is under program control. The light beam is focused onto the entrance slit of the double-grating monochromator which is driven by a motor. The motor also drives a variable resistor connected to a transresistance amplifier to provide a voltage precisely proportional to the wavelength setting of the monochromator. The wavelength range and wavelength change per step are inputted through the teletype. The double grating monochromator is used to achieve very low stray light to insure that the spectral response measured in the absence of bias illumination is indeed the monochromatic response.

The beam emerging from the exit slit of the monochromator is incident on both the cell being tested and a thermopile (Sensors, Inc., Model L22-18) whose sensitivity is wavelength independent (within a few percent, in the range from 450 to 9000 nm, limited by

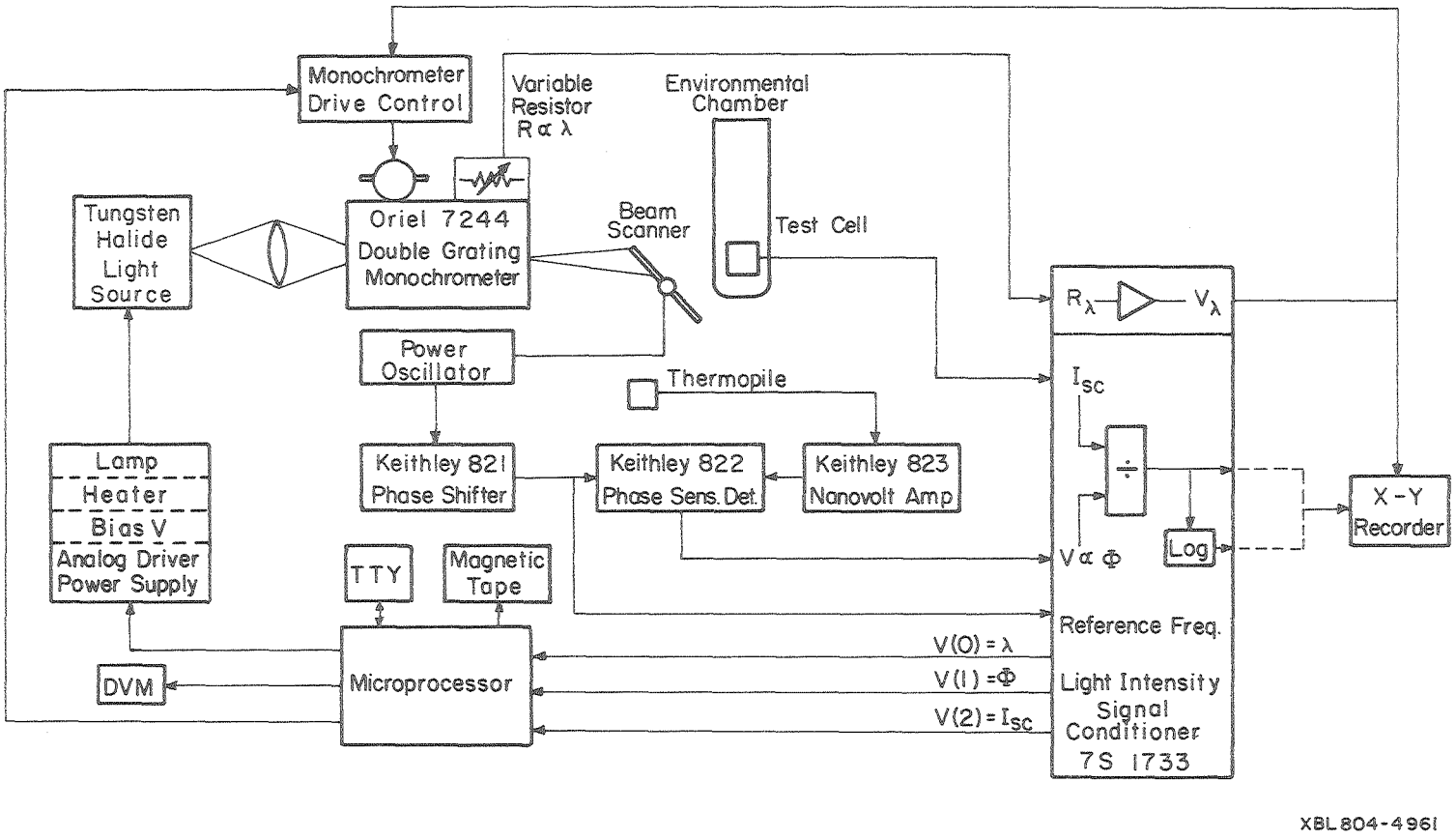

Monochrometer Drive Control
Variable Resistor R α λ
Environmental Chamber
Tungsten Halide Light Source
Oriel 7244 Double Grating Monochrometer
Beam Scanner
Test Cell
Power Oscillator
Thermopile
Lamp Heater Bias V Analog Driver Power Supply
Keithley 821 Phase Shifter
Keithley 822 Phase Sens. Det.
Keithley 823 Nanovolt Amp
TTY
Magnetic Tape
DVM
Microprocessor
V(0) = λ
V(1) = Φ
V(2) = Isc
Rλ
Vλ
Isc
÷
Vα Φ
Log
X-Y Recorder
Reference Freq.
Light Intensity Signal Conditioner 7S 1733
XBL804-4961

Figure 5.10

its CaF_2 window material). The beam is split using a beam scanning galvanometer driven by a power oscillator. This configuration is used to achieve a stable chopping frequency to provide a high signal-to-noise ratio of the short-circuit current and thermopile (light intensity) signals. The thermopile output is amplified by a Keithley "lock-in" amplifier and monitored by the controller as V(1) (see Fig. 5.10). The output of the test cell is connected to an operational amplifier circuit of very low input impedance ($\lesssim 1\Omega$) to approximate short-circuit conditions. This signal is then phase-sensitively detected in the same manner as the thermopile signal. This d.c. voltage, proportional to the a.c. short-circuit current, is recorded by the controller as V(2).

The BASIC program for control of the steady-state spectral response measurements was written so that a set of ten readings of the short-circuit current, with a variable time delay between readings, was taken at a given wavelength. The mean and standard deviation of this data group were then calculated by the microcomputer. A second set of ten readings along with the mean and standard deviation was subsequently taken. The data was considered stable only if the difference between the means of the two sets of readings was less than the sum of the standard deviations; if not, the program initiated another set of measurements. The same procedure was used for obtaining thermopile readings to determine the normalized short-circuit current. The wavelength at which the readings were taken, the average thermopile signal and its standard deviation, the average of the last

twenty stable readings of the short-circuit current and its standard deviation, and normalized short-circuit current were then printed on the teletype and magnetic tape. There was also provision for an on-line plot of the spectral response using an analog divide module and an X-Y recorder as shown in Fig. 5.10.

Also shown in Fig. 5.10 are the components to be used for I-V-T measurements. The environmental chamber for the test cell consists of an evacuated sample holder immersed in a liquid nitrogen dewar with a heater and thermocouple to allow program control of the sample temperature. An available bias voltage from 0 to 1V is shown in the Analog Driver Power Supply. Difficulties in producing cells of low enough series resistance has limited the usage of the I-V-T measurement portion of the apparatus.

Figure 5.11 shows the room temperature front-wall mode spectral response of cell 6167-1. This measurement indicates that the Cu_xS layer was too thin since there was a large mixed crystal response at ~ 400 nm in spite of the good long wavelength response; this contributes to the low measured short-circuit current. The shape of the long wavelength response indicates good stoichiometry of the Cu_xS; a moderately thick chalcocite (Cu_2S) layer, however, would be opaque at 400 nm. Spectral response measurements of cells for which the Cu_xS was formed by reactive sputtering showed very similar characteristics with a large response from the CdS or (Cd,Zn)S.

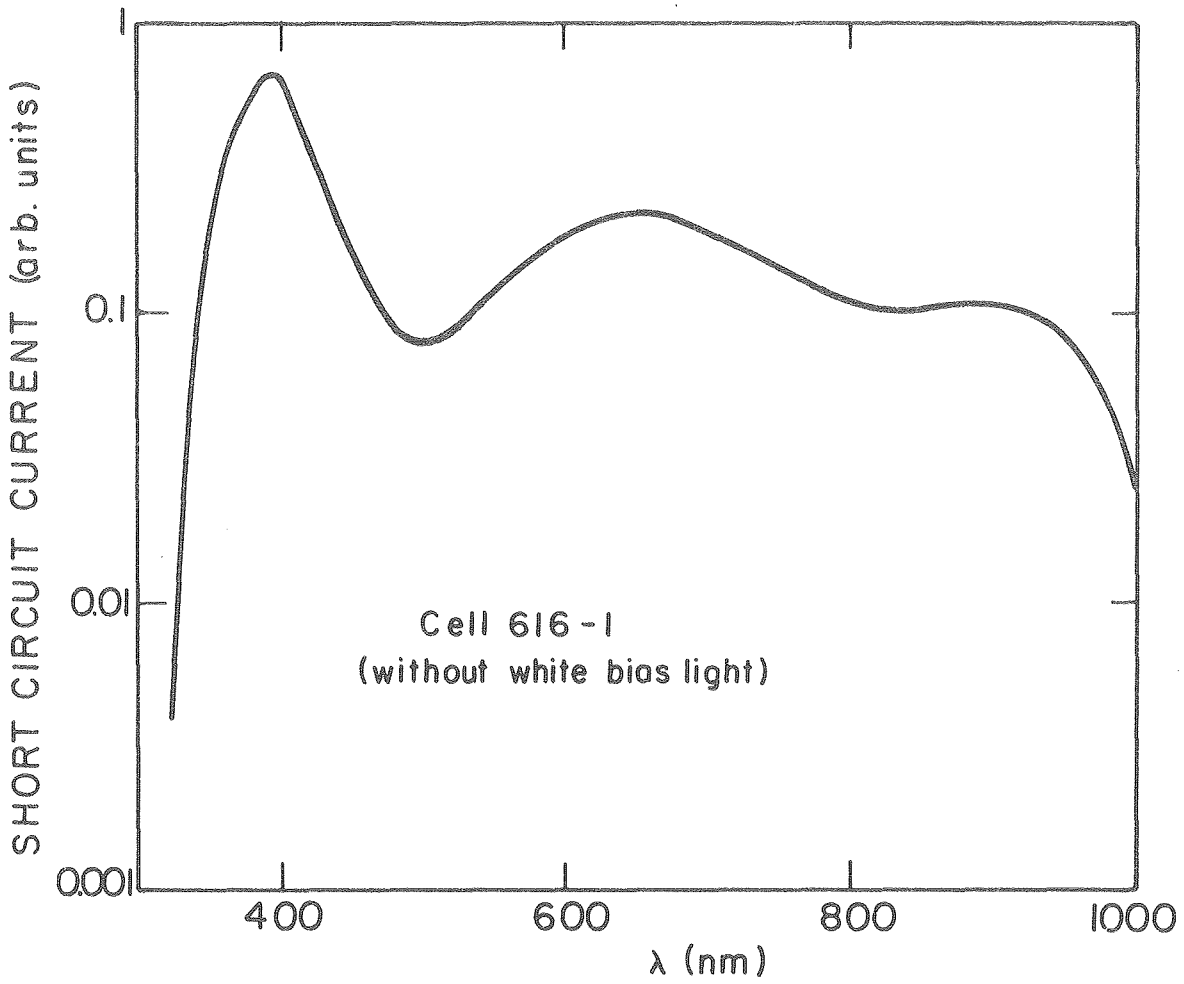

SHORT CIRCUIT CURRENT (arb. units)
1
0.1
0.01
0.001
Cell 616-1
(without white bias light)
400
600
800
1000
λ (nm)
XBL 777-5844

Figure 5.11

6. Discussion and Recommendations

As stated earlier in this report, the objective of this program was to better understand some of the factors affecting the efficiency of Cu_xS/CdS and Cu_xS/(Cd,Zn)S solar cells. In order to reduce the number of variables, the simplest configuration was used, i.e., a planar interface between single crystal CdS and (Cd,Zn)S films and epitaxial Cu_xS. This situation is equivalent to studying the smallest unit of a polycrystalline cell, i.e., a single grain. However, even in this case, cell efficiency is influenced by many variables as illustrated in this report. The most important of these and our recommendations as to their control are outlined below.

6.1 Film Growth

A number of different single crystal semiconductor surfaces and orientations were used as substrates for the heteroepitaxial growth of CdS and (Cd,Zn)S; each of which presented its own unique set of problems. Much effort was devoted towards solving these problems in order to obtain good single crystal films which could be used to form heterojunction cells and also be characterized after each processing step. This was considered an essential aspect of the program because detailed information concerning growth conditions and defect structure could be correlated with device performance.

It was found experimentally that both the composition and growth rate of (Cd,Zn)S single crystal films depended very strongly on the ratio of CdS to ZnS evaporated as shown in Figs. 3.12-3.14. These graphs may be used as guidelines for the vapor growth of (Cd,Zn)S thin

films of a desired composition. These same experiments also indicated the importance of eliminating cross-contamination between the CdS and ZnS sources. It should also be noted that for lateral uniformity of the film composition, due to the higher diffusivity of Cd, temperature gradients across the substrate surface must be avoided.

It was found that GaAs substrates were unsuitable for front-wall test cell construction because of the non-ohmic junction with CdS. Film growth experiments on the various (111) Ga or As faces and off-(111) orientations were of interest, however, in providing information about growth rates and crystalline perfection. TEM studies and Hall Effect experiments were conducted on these films to try to identify effects of structural defects on electrical properties. A large part of this information was transferred to the growth of CdS and (Cd,Zn)S on (111) n-Ge which does form an ohmic isotype heterojunction.

Processing parameters for the deposition of single crystal CdS on Ge substrates were determined and reproducible growth was attained. For (Cd,Zn)S film growth it was found that an intermediate layer of pure CdS was necessary. Films grown on Ge substrates were used for TEM examination and cell fabrication.

6.2 Defect Structure

Recent improvement in the preparation technique of thin foils for electron microscopy has made a detailed structural characterization of the films possible. It was shown that a relatively high density of dislocations exists in the single crystal CdS films. Loose

dislocation networks parallel to the plane of the foil in or near the CdS/substrate interface were found in all the samples investigated. Closer to the top surface of the film a lower density of steeply inclined dislocations was present. A network of misfit dislocations, as shown in Fig. 4.1a, is necessary to accommodate the mismatch between the substrate and the film.

Inclined dislocations perpendicular to the substrate as shown in Figs. 4.1b and c have no role in the accommodation of the lattice mismatch. Their existence was probably due to the growing together of misfitting islands of CdS during the early stages of film growth. If this is indeed the case, then some dislocation lines are likely to traverse the entire thickness of the CdS film, providing an easy diffusion path for Cu during the heterojunction formation or subsequent heat treatments. As a result, short circuiting of the cell, as experimentally observed in some cases, may occur. A more conclusive check of this mechanism would be the examination of a cross-section of the CdS/substrate interface in TEM. Long inclined dislocations and their effects on the structure of the Cu_xS/CdS heterojunction could then be studied.

While the TEM micrographs such as Figs. 4.10 and 4.12 show the structural similarity between Cu_xS films that were formed on CdS by reactive sputtering and by the ion exchange methods, much more detailed work is necessary to determine the composition and structure of the various Cu_xS phases characteristic of a given fabrication process. The transmission electron microscope is unique in its

ability to identify crystal structures locally while at the same time providing detailed morphological information. An example of the resolution with which structures may be observed is shown in Fig. 4.14. Using similar techniques the study of the heterojunction would be possible allowing for a detailed analysis of its interface structure. Valuable direct information could thus be obtained about the perfection of the heterojunction, localized defects which may act as trapping or recombination centers, the mechanism of the ion exchange reaction itself, and the influence of defects inherited from the CdS film. This preliminary study demonstrates that further work of this type could contribute to a more fundamental understanding of the role of defects in determining the properties of the Cu_xS/CdS and Cu_xS/(Cd,Zn)S cells.

Although the major part of this study focused on single crystal films, many of the findings also apply to polycrystals. In particular, it is believed that a basic structural understanding of the kinds of defects present at or near the junction as provided by the techniques of TEM will be found to be essential to the successful development of a technology for the reproducible growth of high-efficiency, long life-time cells. The process of degradation could be studied "in situ" in a TEM equipped with an environmental cell.

6.3 Test Device Performance

Test devices were fabricated to determine the effects of different processing parameters on resulting structural and electrical properties. Hall Effect experiments showed electron mobilities in our vapor grown CdS films which are comparable to other published results. This indicates that the dislocations observed in these grown films did not seriously affect the bulk properties. However, as noted in the previous section, these same dislocations may be extremely detrimental during the heterojunction formation or heat treatment and therefore adversely affect cell performance.

The current voltage characteristics of cells formed by the ion-exchange and reactive sputtering processes showed low short-circuit current densities. This was partly due to the inadequate thickness of the Cu_xS resulting in lower absorption of photons as observed in the spectral response measurements. Cells formed by the ion-exchange method also had low shunt resistances resulting in poor fill factors. One possible cause is the role of inclined dislocations in providing low resistance shunting paths. To improve the performance of these test cells several aspects of the cell construction could be altered. The total series resistance of the cell could be lowered by doping the CdS or (Cd,Zn)S films with In and also by the development of a better front contact structure to prevent current crowding. Another critical improvement would be the optimization of Cu_xS thickness and stoichiometry.

The cell performance predicted on the basis of bulk electronic properties of CdS, (Cd,Zn)S and Cu_xS and their idealized interface exceeds that found in any real device made to date. It is increasingly clear that other factors such as the structural perfection of the films and heterojunction interface are limiting the cell efficiency. A more extensive high resolution study of the defect populations in single crystal and polycrystalline Cu_xS/CdS and Cu_xS/(Cd,Zn)S photovoltaic devices is essential to provide the kind of information that will be necessary to identify steps in the present techniques for fabricating cells that need improvement.

Much of the effort of this program was spent on overcoming problems encountered in the preparation of good quality single crystal films and the preparation of undamaged electron microscope specimens for their characterization. Now that these problems have been solved, it is clear that further work can achieve meaningful correlations between structural information and cell performance.

7. ACKNOWLEDGEMENTS

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